#8

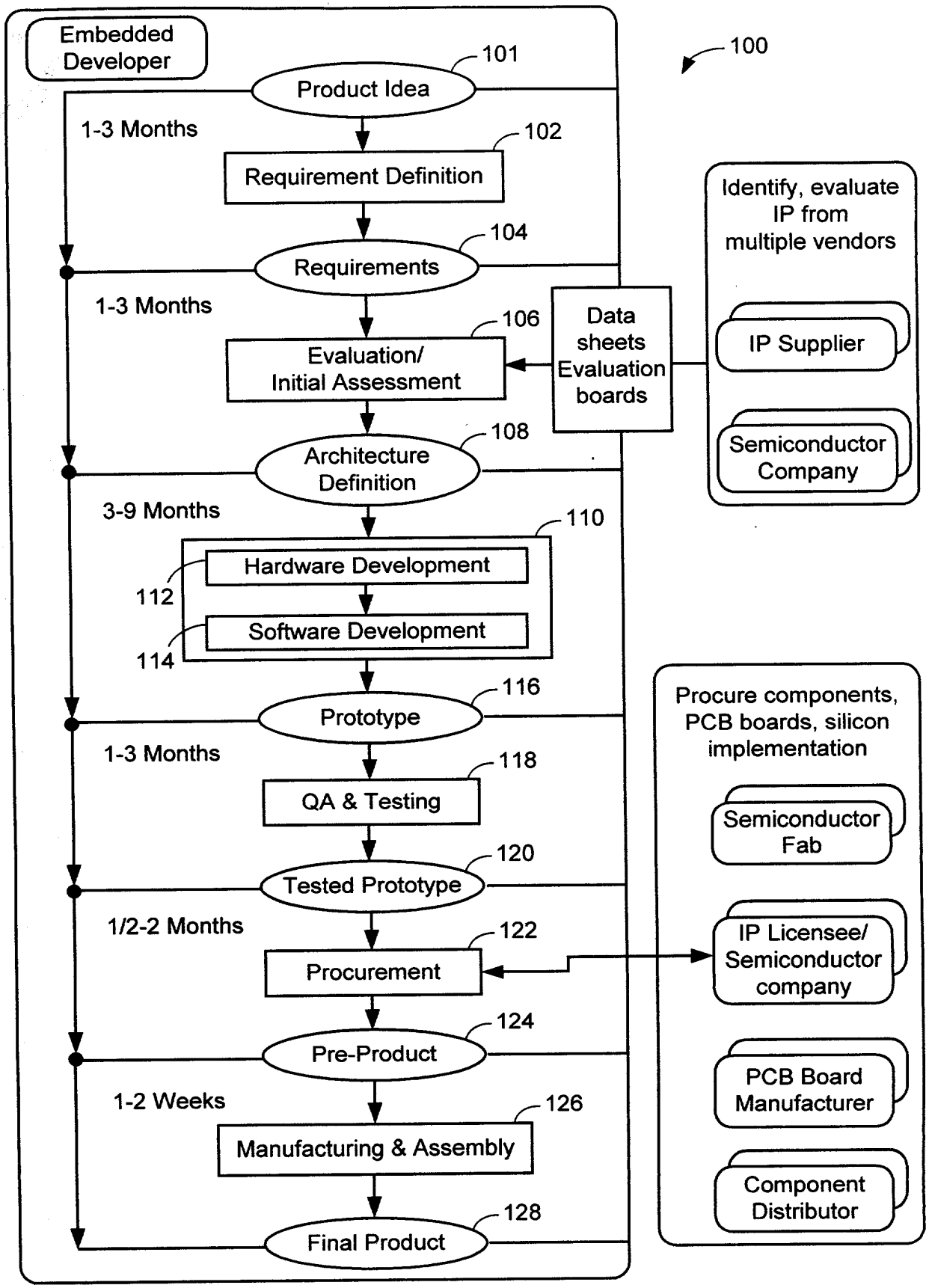

Fig. 1 (Prior Art)

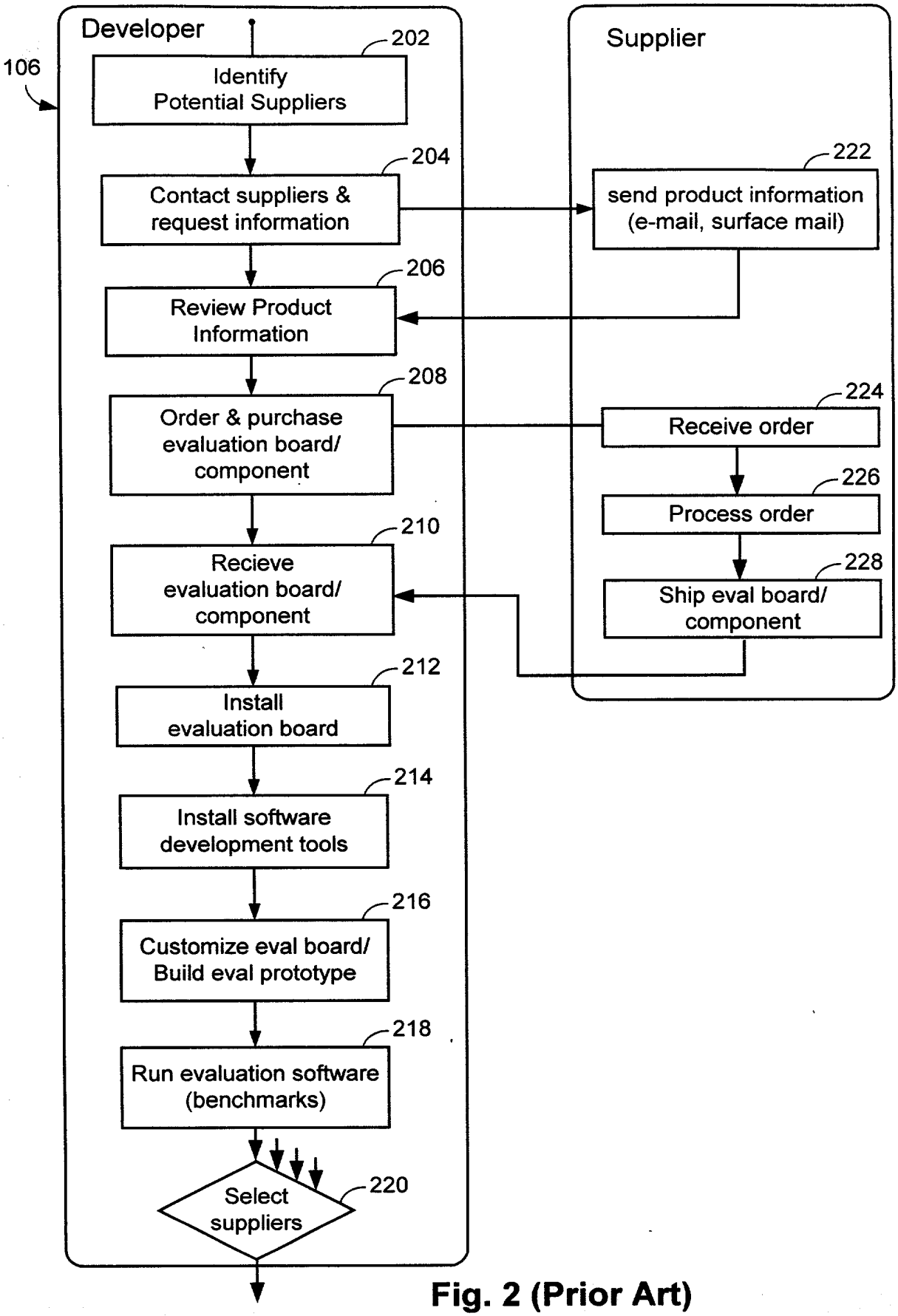

Fig. 2 (Prior Art)

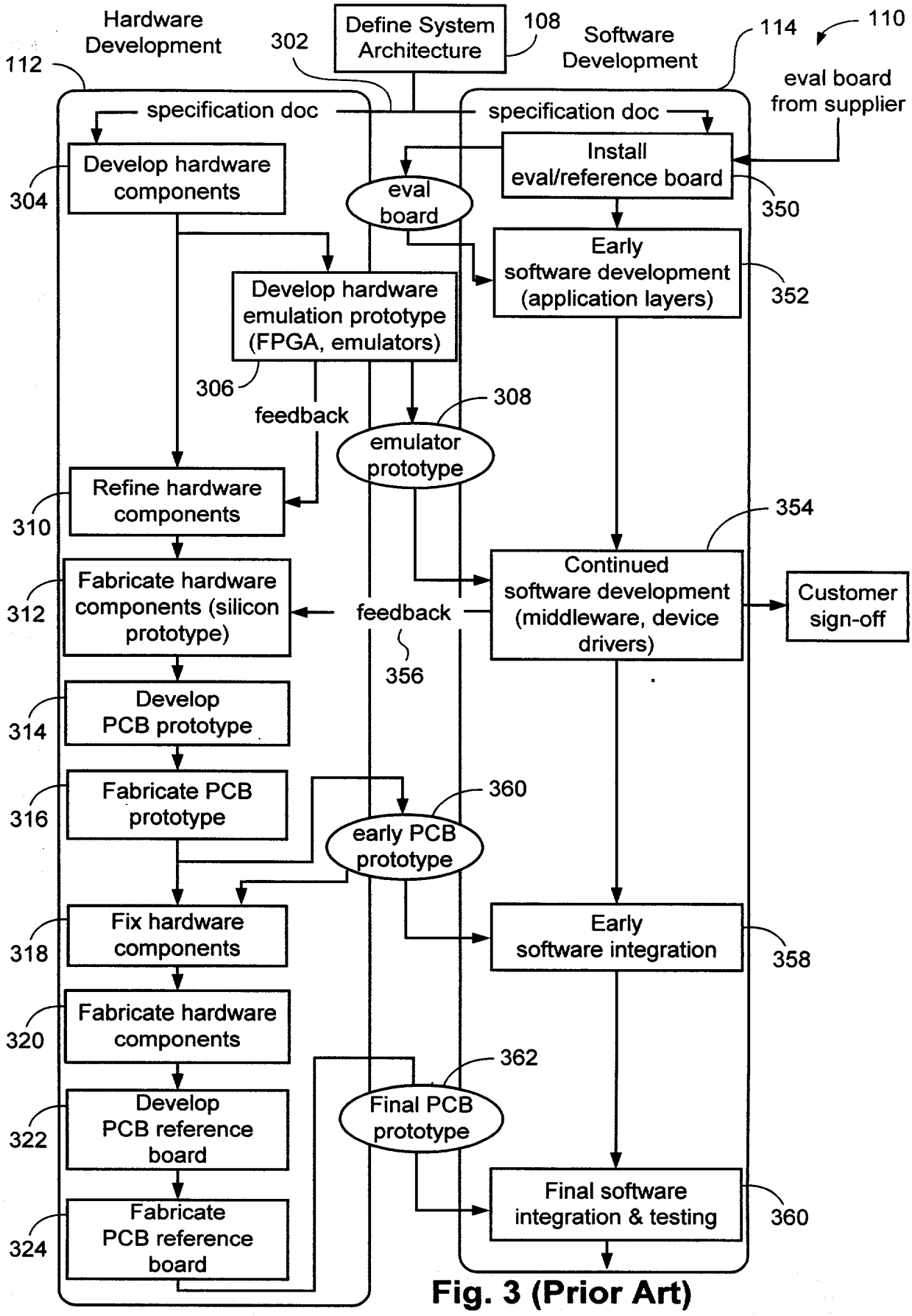

Fig. 3 (Prior Art)

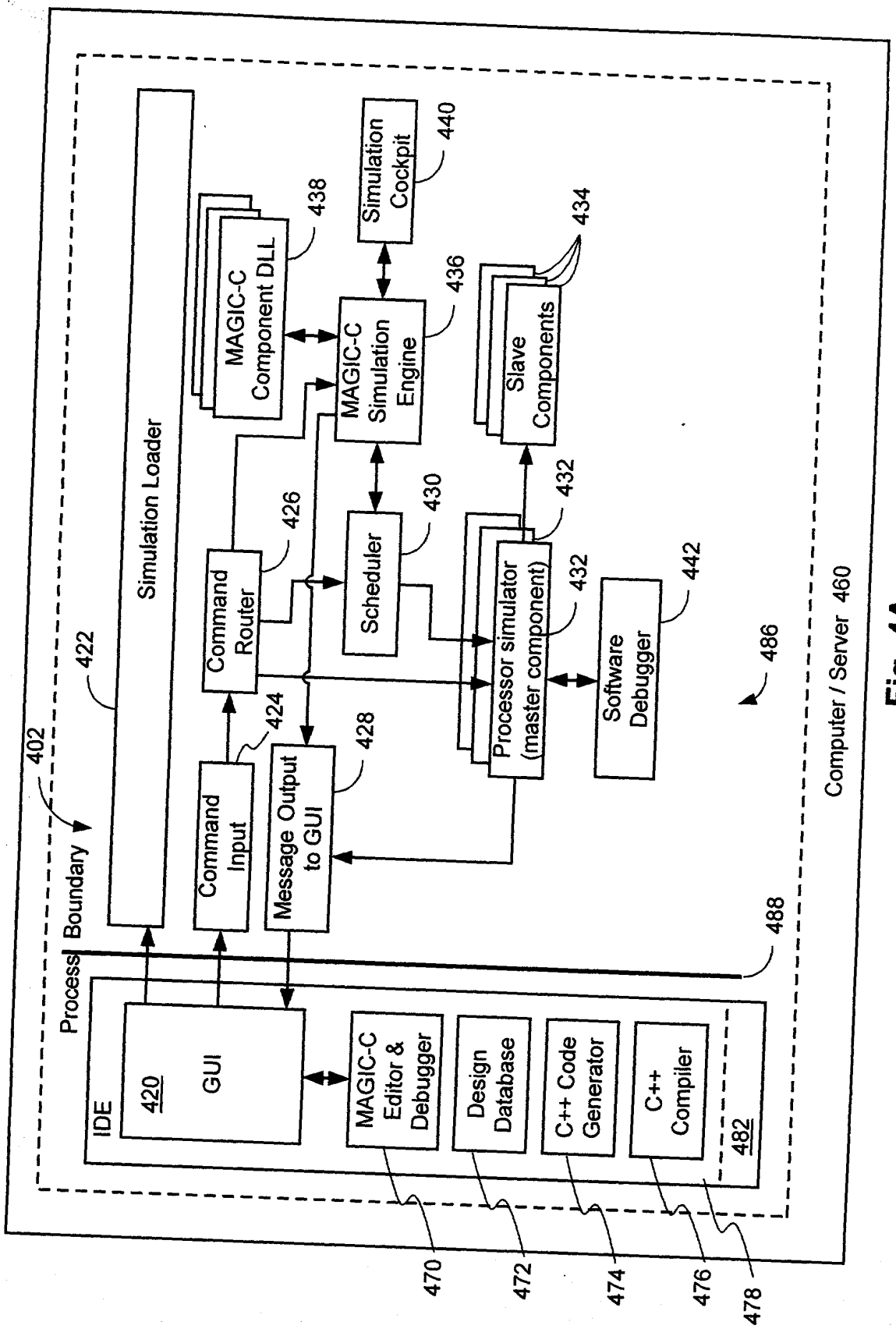
Computer / Server 460
Process Boundary
402
IDE
420
GUI
Simulation Loader
422
Command Input
424
Message Output to GUI
428
Command Router
426
Scheduler
430
Processor simulator (master component)
432
Software Debugger
442
MAGIC-C Component DLL
438
MAGIC-C Simulation Engine
436
Simulation Cockpit
440
Slave Components
434
MAGIC-C Editor & Debugger
Design Database
C++ Code Generator
C++ Compiler
482
486
488
470
472
474
476
478

Fig. 4A

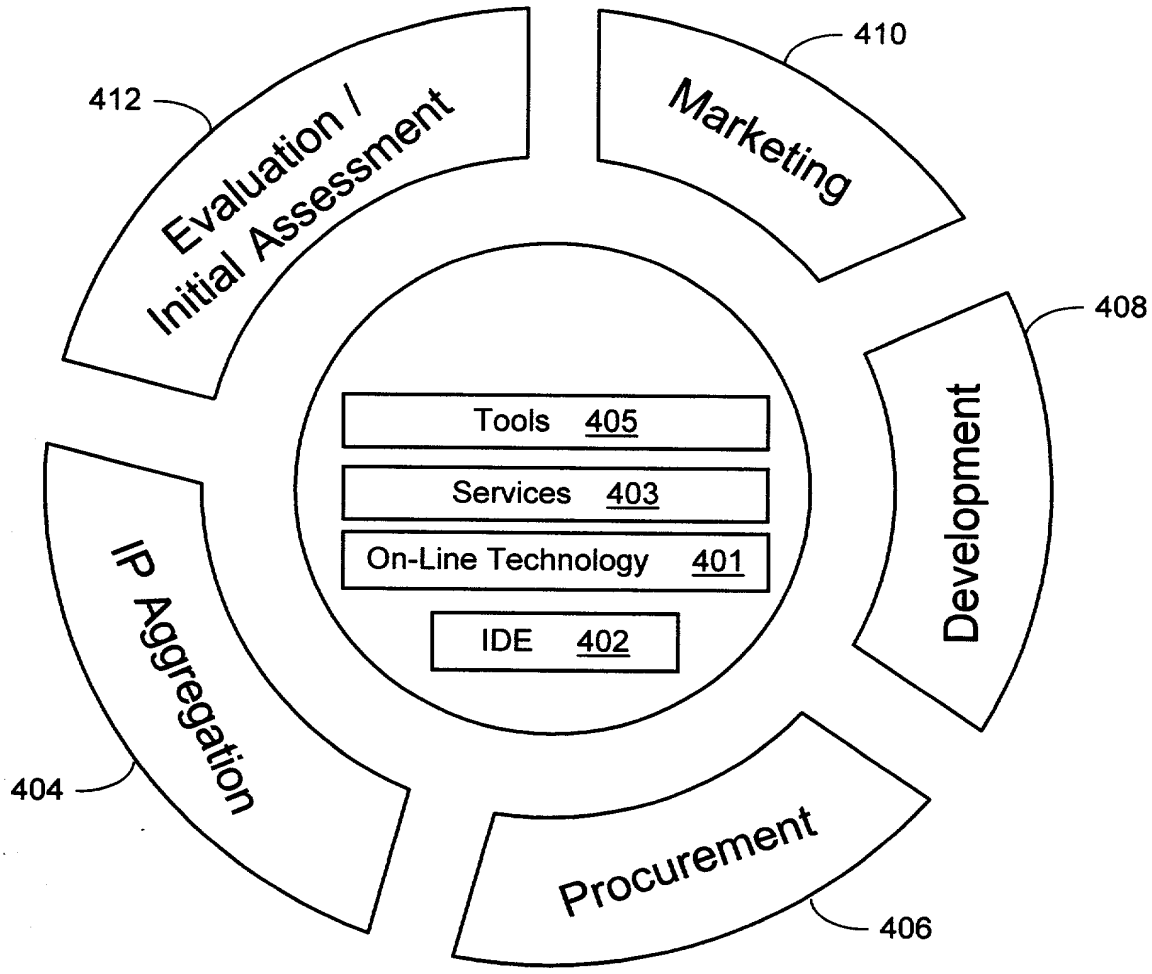
410
412
Evaluation / Initial Assessment
Marketing
408
Development
Tools 405
Services 403
On-Line Technology 401
IDE 402
IP Aggregation
404
Procurement
406

Fig. 4B

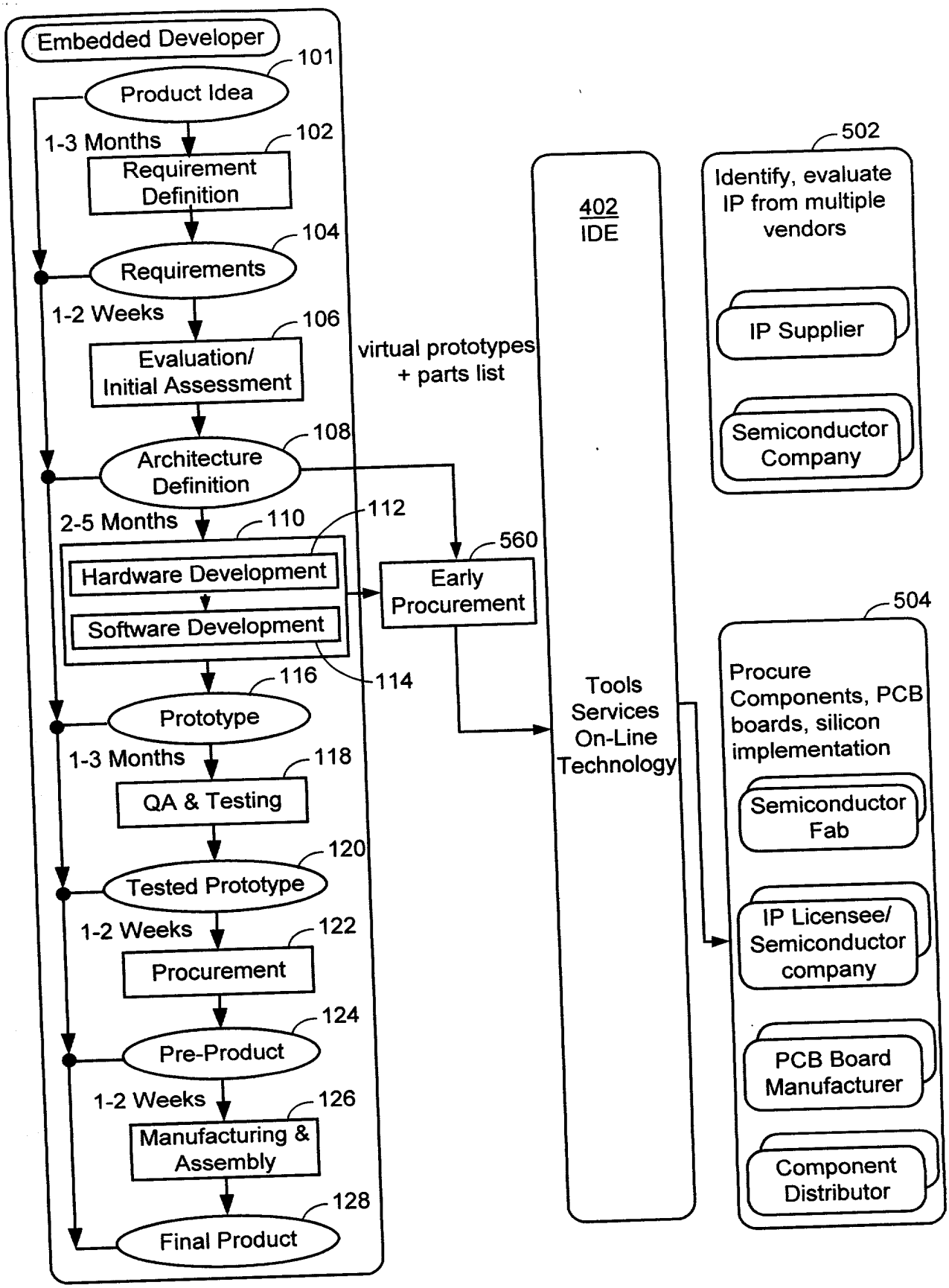
Embedded Developer
101
Product Idea
1-3 Months
102
Requirement Definition
104
Requirements
1-2 Weeks
106
Evaluation/ Initial Assessment
108
Architecture Definition
2-5 Months
110
112
Hardware Development
Software Development
114
116
Prototype
1-3 Months
118
QA & Testing
120
Tested Prototype
1-2 Weeks
122
Procurement
124
Pre-Product
1-2 Weeks
126
Manufacturing & Assembly
128
Final Product
virtual prototypes + parts list
560
Early Procurement
402
IDE
Tools
Services
On-Line
Technology
502
Identify, evaluate IP from multiple vendors
IP Supplier
Semiconductor Company
504
Procure Components, PCB boards, silicon implementation
Semiconductor Fab
IP Licensee/ Semiconductor company
PCB Board Manufacturer
Component Distributor

Fig. 5

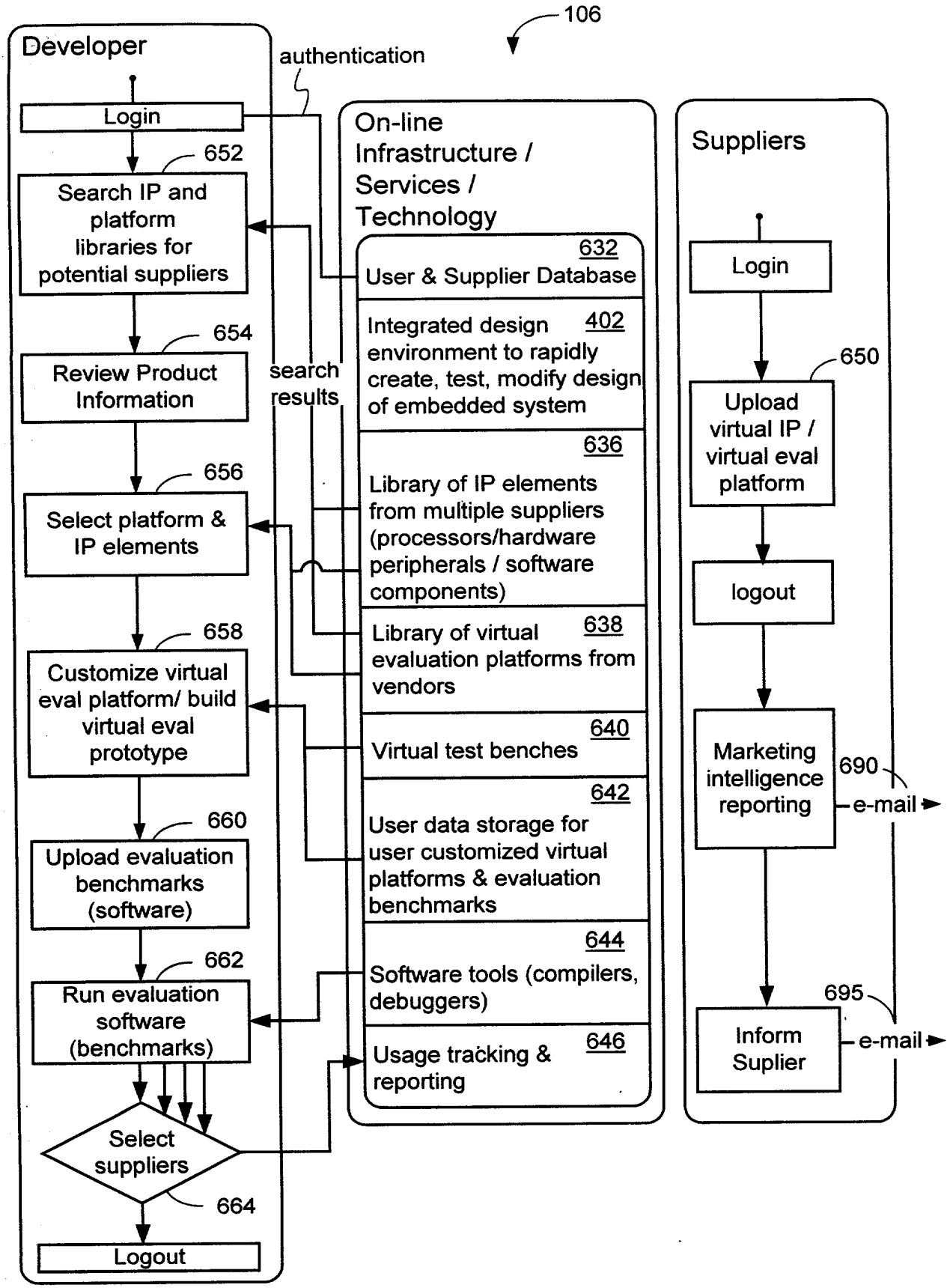
106
Developer
authentication
Login
652
Search IP and platform libraries for potential suppliers
654
Review Product Information
656
Select platform & IP elements
658
Customize virtual eval platform/ build virtual eval prototype
660
Upload evaluation benchmarks (software)
662
Run evaluation software (benchmarks)
Select suppliers
664
Logout
search results
On-line Infrastructure / Services / Technology
632
User & Supplier Database
Integrated design environment to rapidly create, test, modify design of embedded system 402
636
Library of IP elements from multiple suppliers (processors/hardware peripherals / software components)
638
Library of virtual evaluation platforms from vendors
640
Virtual test benches
642
User data storage for user customized virtual platforms & evaluation benchmarks
644
Software tools (compilers, debuggers)
646
Usage tracking & reporting
Suppliers
Login
650
Upload virtual IP / virtual eval platform
logout
Marketing intelligence reporting
690
e-mail
695
Inform Suplier
e-mail

Fig. 6

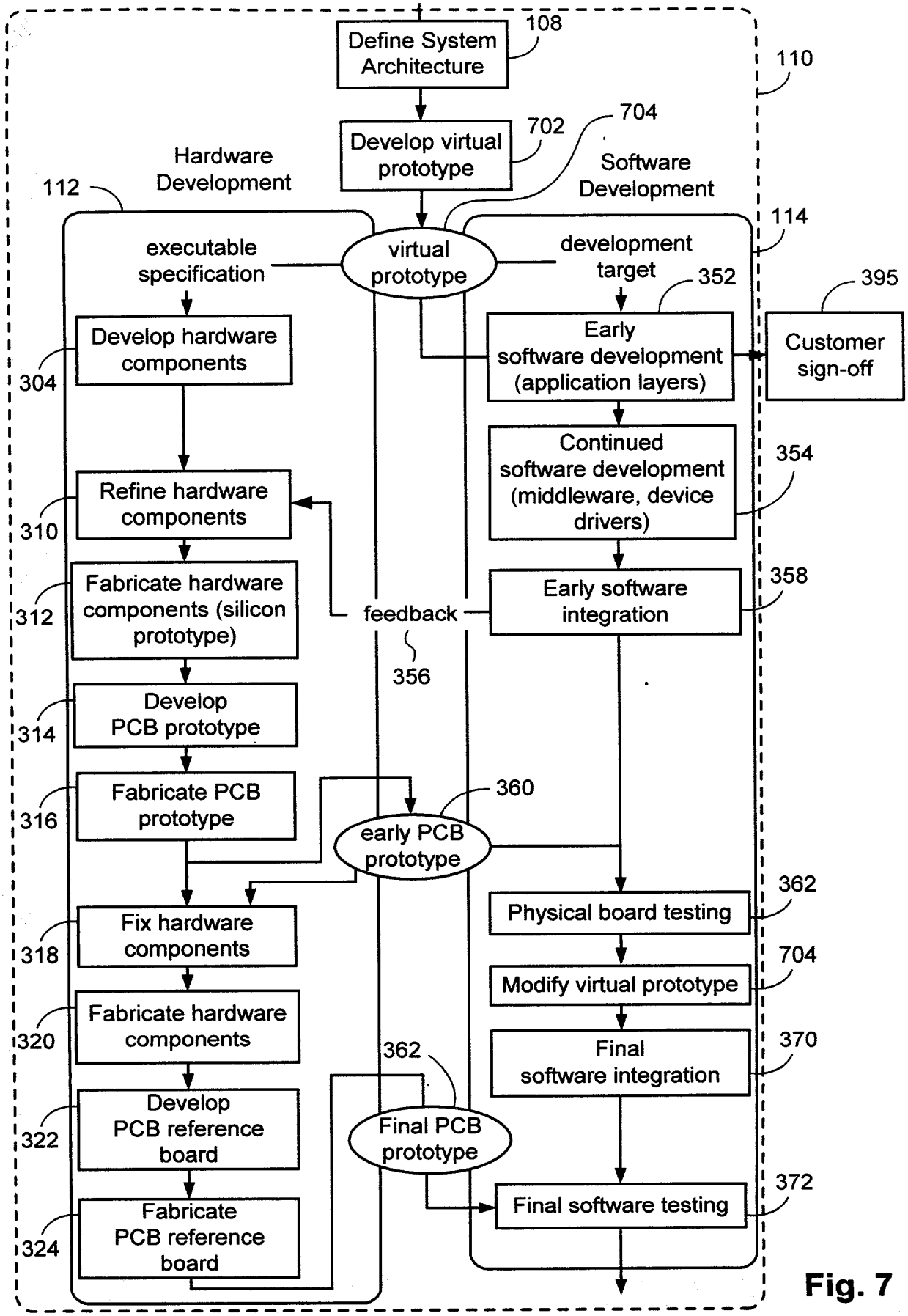
Define System Architecture
108
110
Develop virtual prototype
702
704
Hardware Development
Software Development
112
114
executable specification
virtual prototype
development target
352
395
Develop hardware components
304
Early software development (application layers)
Customer sign-off
Continued software development (middleware, device drivers)
354
Refine hardware components
310
Fabricate hardware components (silicon prototype)
312
feedback
356
Early software integration
358
Develop PCB prototype
314
Fabricate PCB prototype
316
360
early PCB prototype
362
Physical board testing
Fix hardware components
318
704
Modify virtual prototype
Fabricate hardware components
320
Final software integration
370
362
Develop PCB reference board
322
Final PCB prototype
Fabricate PCB reference board
324
372
Final software testing

Fig. 7

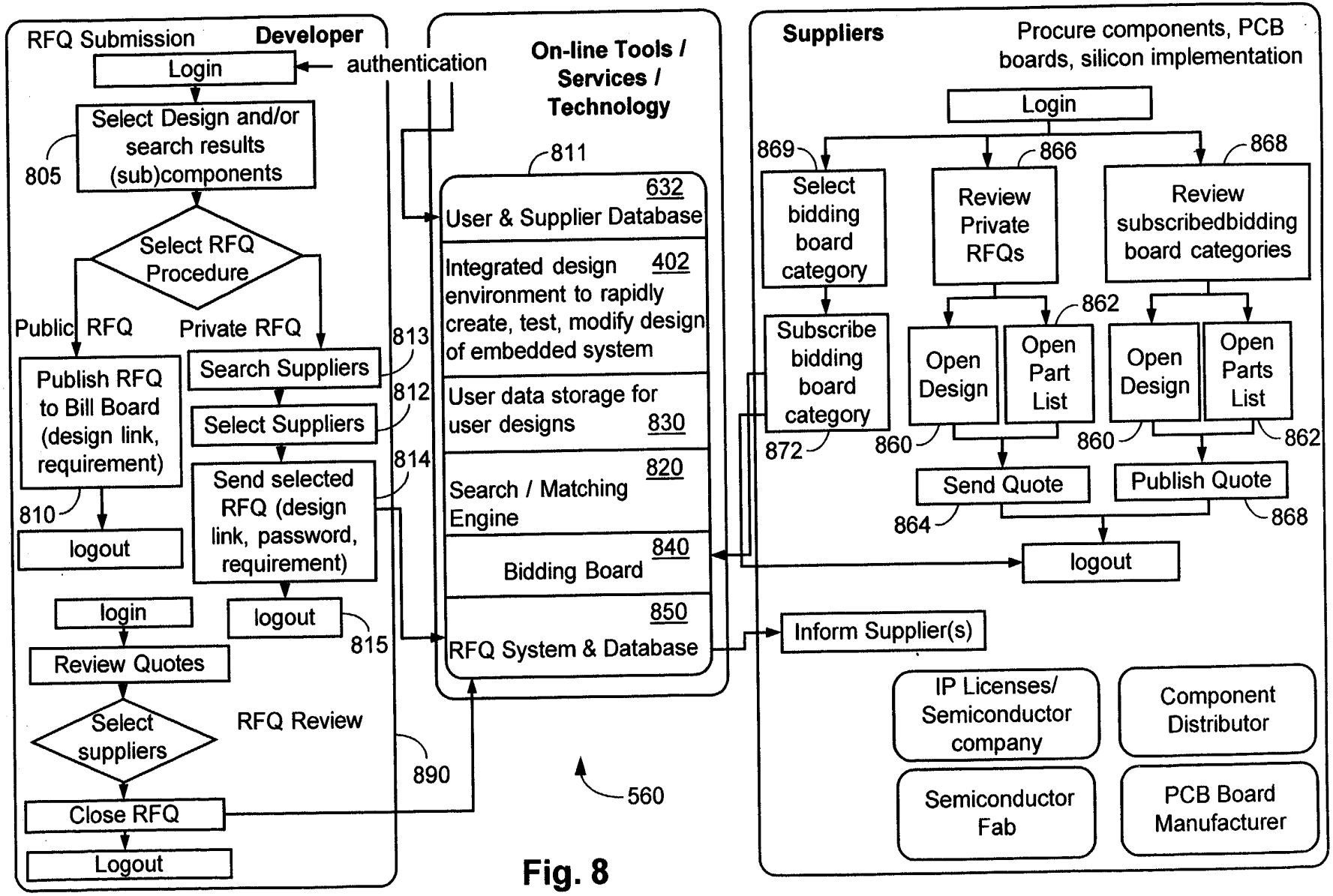

Fig. 8

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
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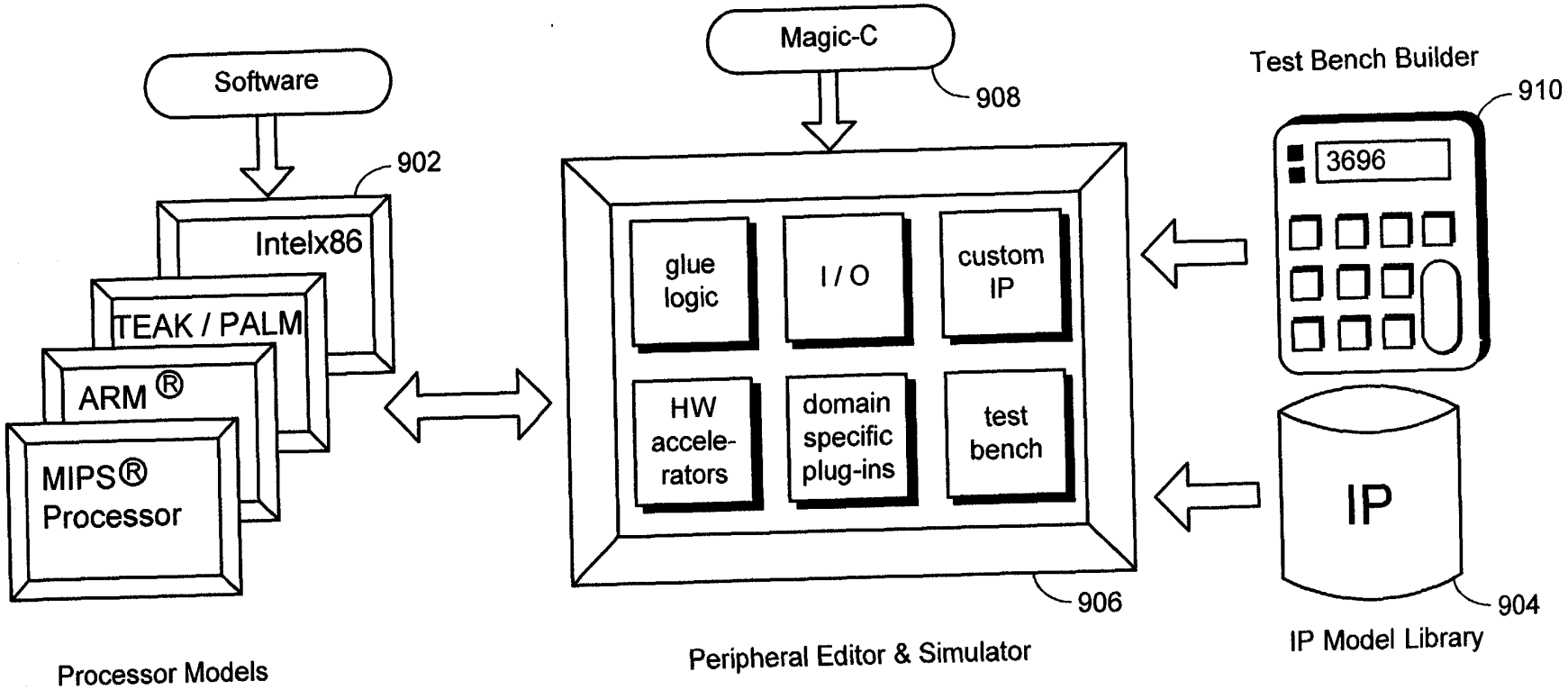

Fig. 9

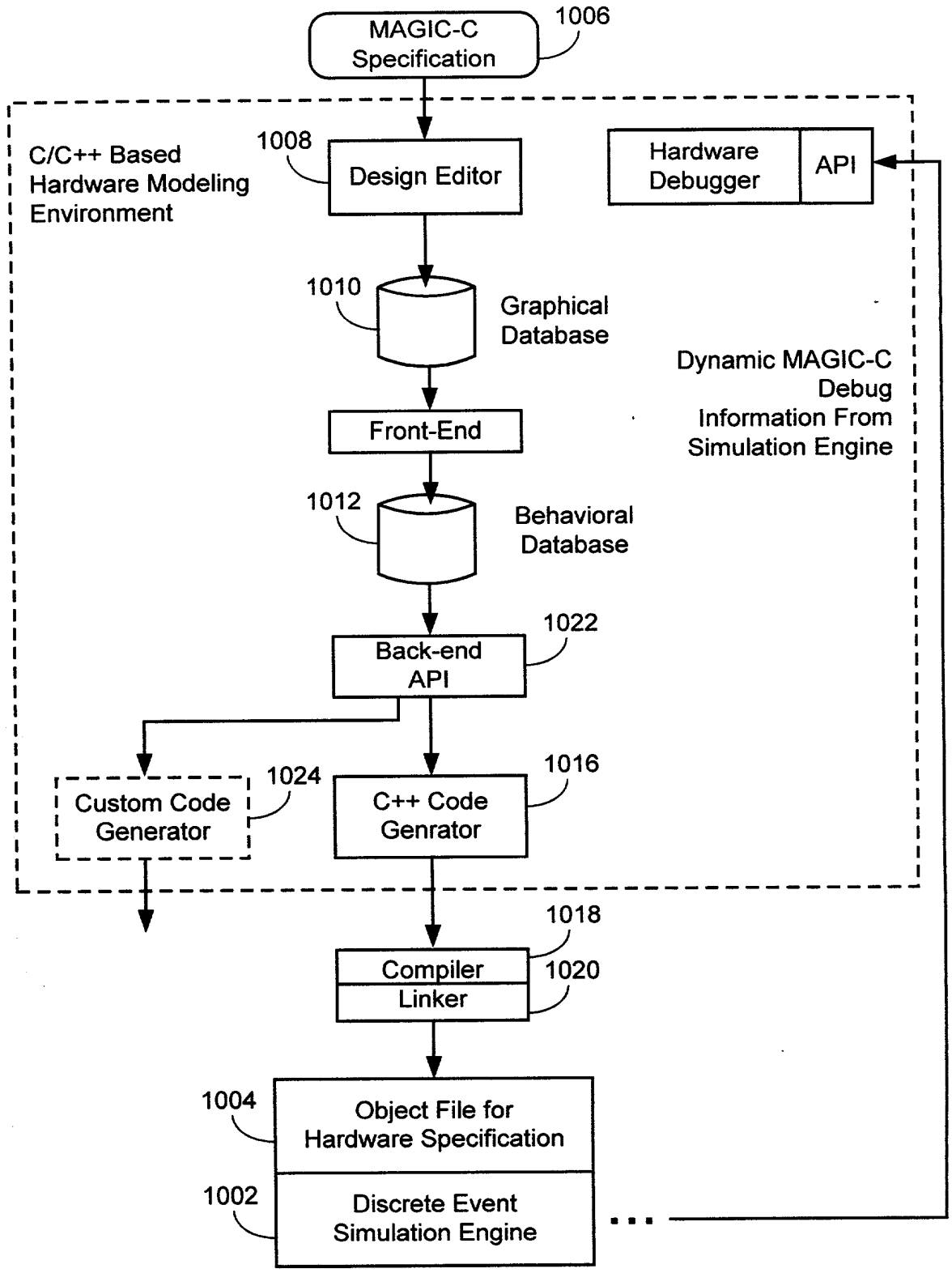
MAGIC-C Specification
1006
C/C++ Based Hardware Modeling Environment
1008
Design Editor
Hardware Debugger
API
1010
Graphical Database
Dynamic MAGIC-C Debug Information From Simulation Engine
Front-End
1012
Behavioral Database
1022
Back-end API
1024
Custom Code Generator
1016
C++ Code Genrator
1018
Compiler
1020
Linker
1004
Object File for Hardware Specification
1002
Discrete Event Simulation Engine

Fig. 10

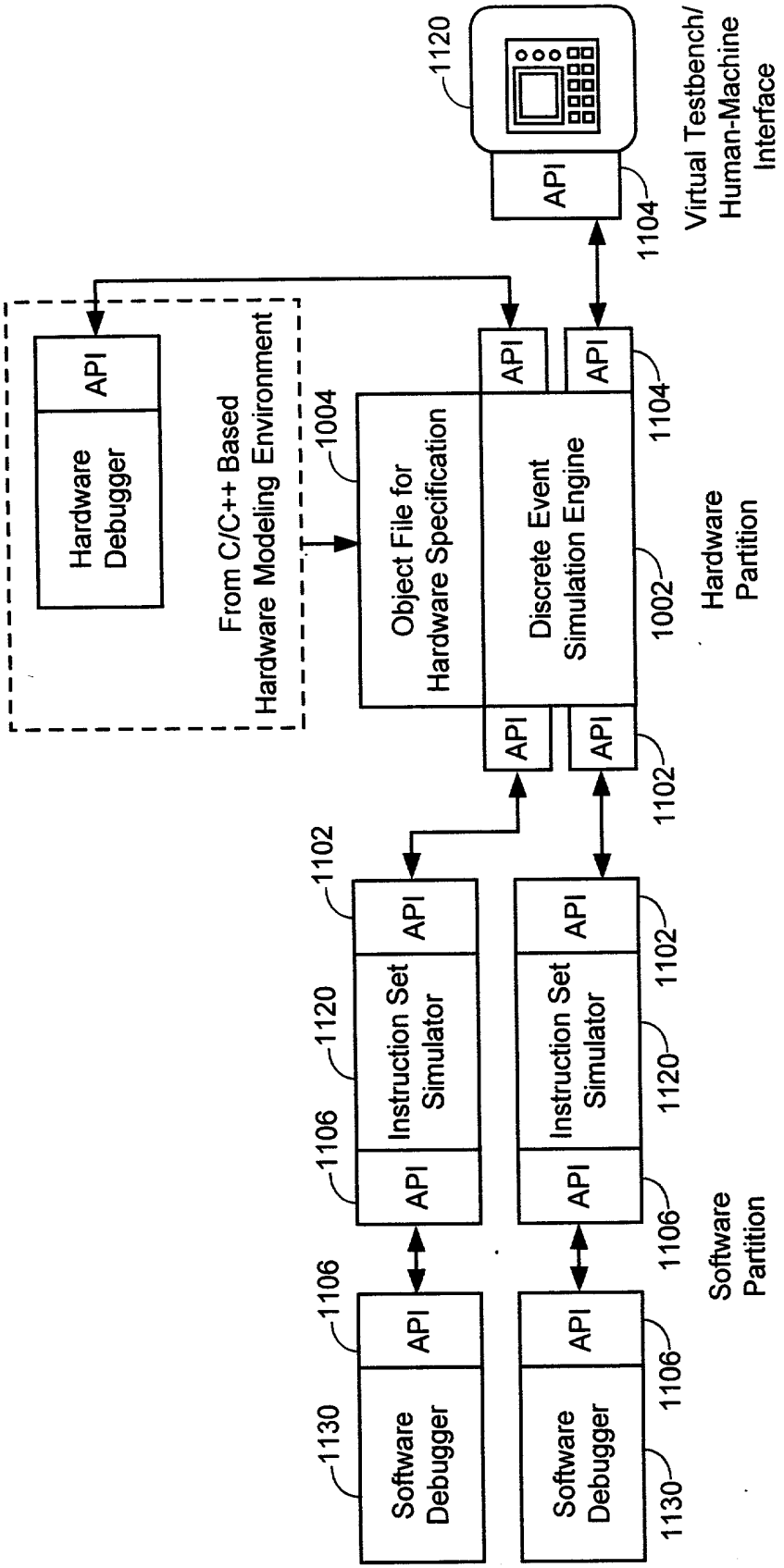
1120
API
1104
Virtual Testbench/
Human-Machine
Interface
API
Hardware
Debugger
From C/C++ Based
Hardware Modeling Environment
1004
Object File for
Hardware Specification
API
API
1104
Discrete Event
Simulation Engine
1002
Hardware
Partition
API
API
1102
1102
API
Instruction Set
Simulator
1120
1106
API
1102
API
Instruction Set
Simulator
1120
1106
API
API
1106
Software
Debugger
1130
API
1106
Software
Debugger
1130
Software
Partition

Fig. 11

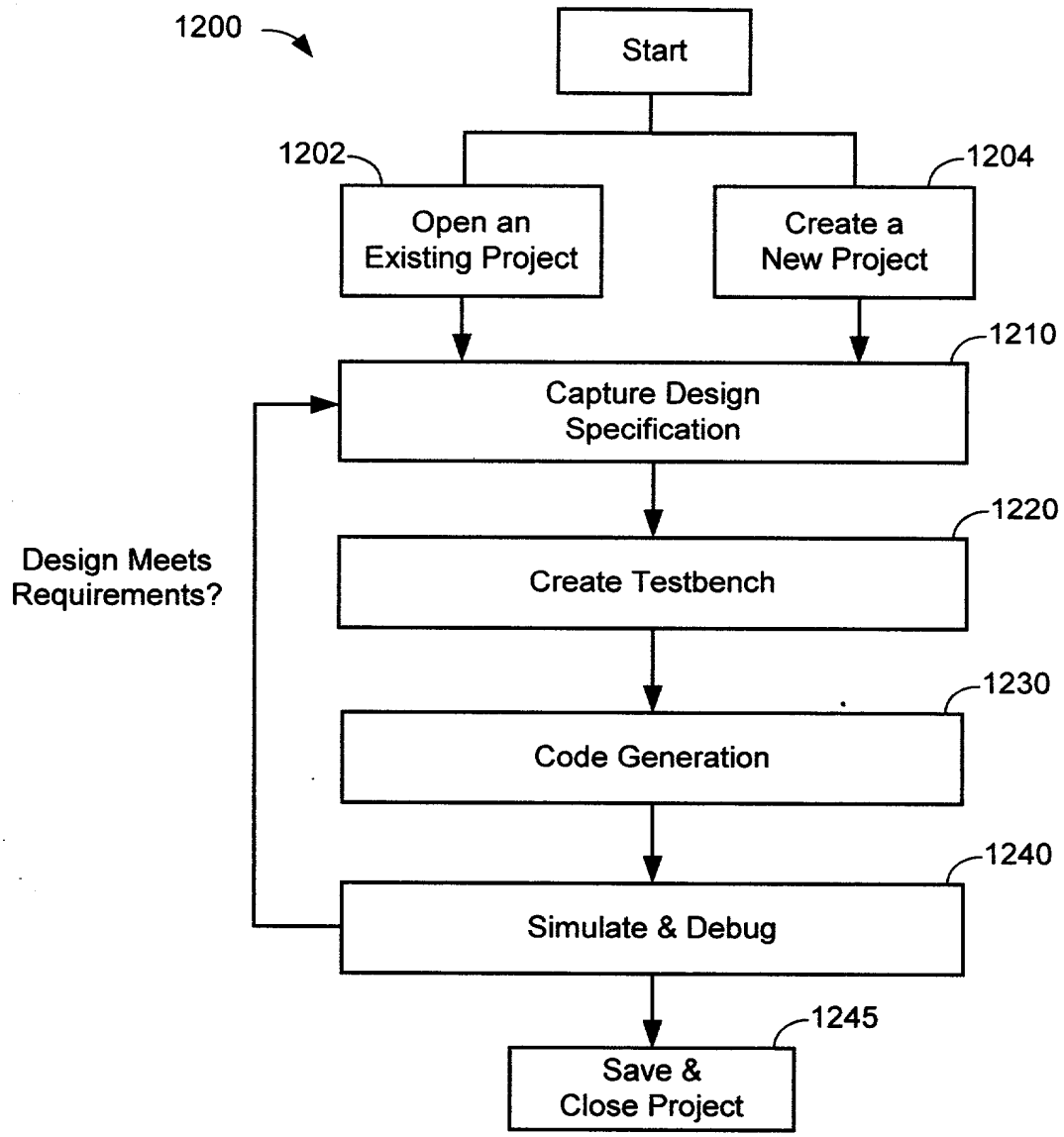
1200
Start
1202
Open an Existing Project
1204
Create a New Project
1210
Capture Design Specification
1220
Create Testbench
1230
Code Generation
1240
Simulate & Debug
1245
Save & Close Project
Design Meets Requirements?

Fig. 12

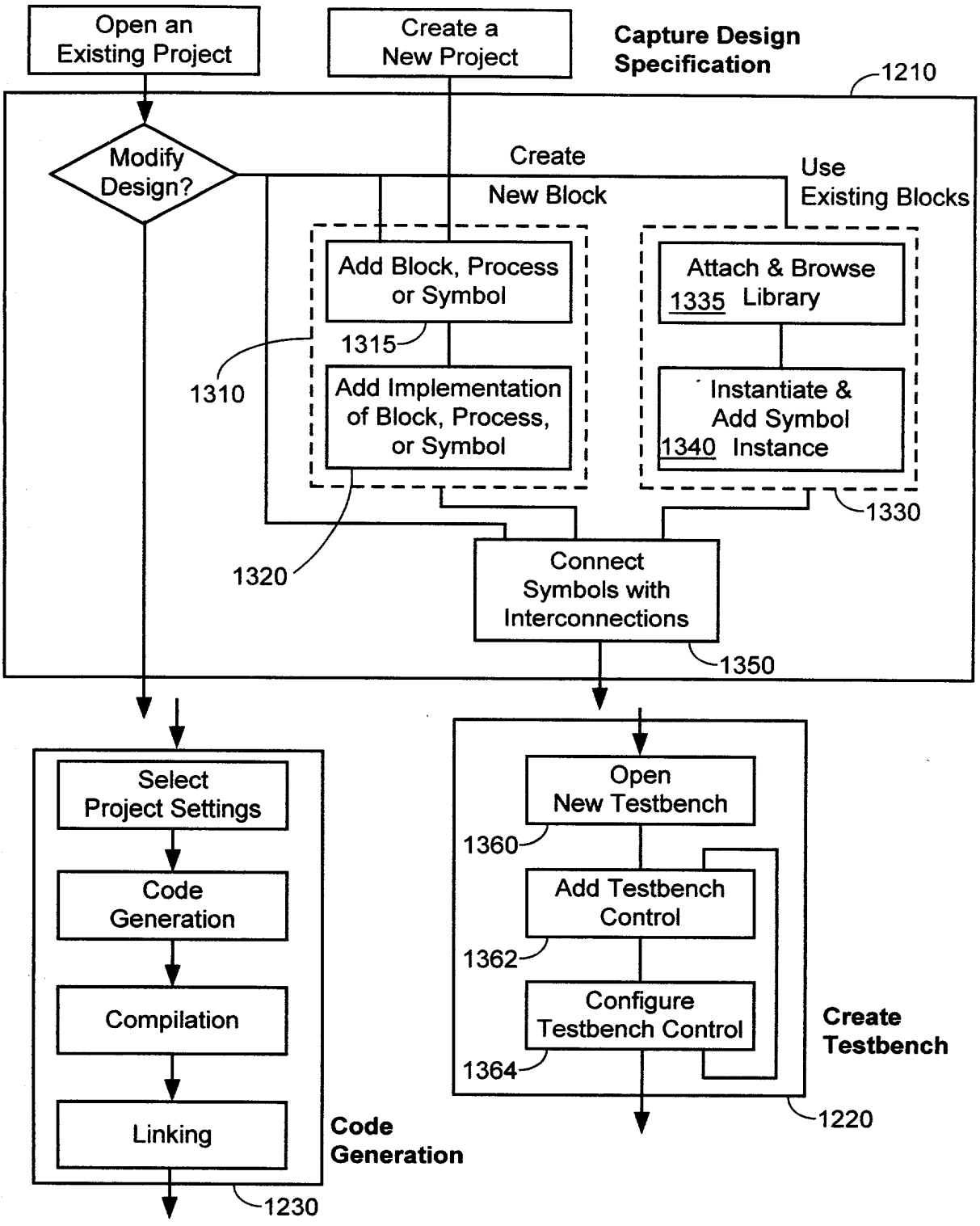
Open an Existing Project
Create a New Project
Capture Design Specification
1210
Modify Design?
Create New Block
Use Existing Blocks
Add Block, Process or Symbol
1315
1310
Add Implementation of Block, Process, or Symbol
Attach & Browse 1335 Library
Instantiate & Add Symbol 1340 Instance
1330
1320
Connect Symbols with Interconnections
1350
Select Project Settings
Code Generation
Compilation
Linking
Code Generation
1230
Open New Testbench
1360
Add Testbench Control
1362
Configure Testbench Control
1364
Create Testbench
1220

Fig. 13

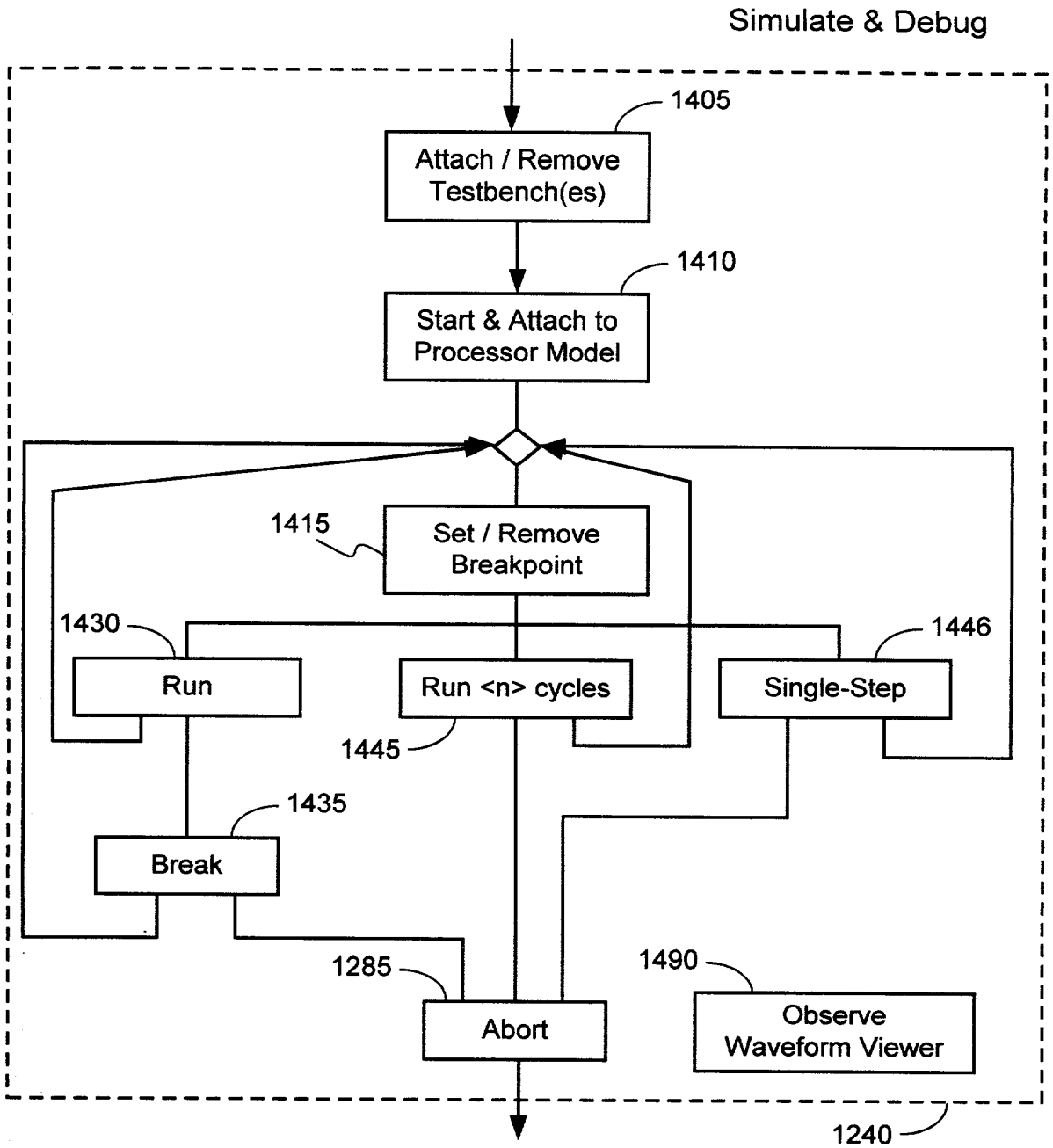
Simulate & Debug
1405
Attach / Remove Testbench(es)
1410
Start & Attach to Processor Model
1415
Set / Remove Breakpoint
1430
Run
Run <n> cycles
1445
1446
Single-Step
1435
Break
1285
Abort
1490
Observe Waveform Viewer
1240

Fig. 14

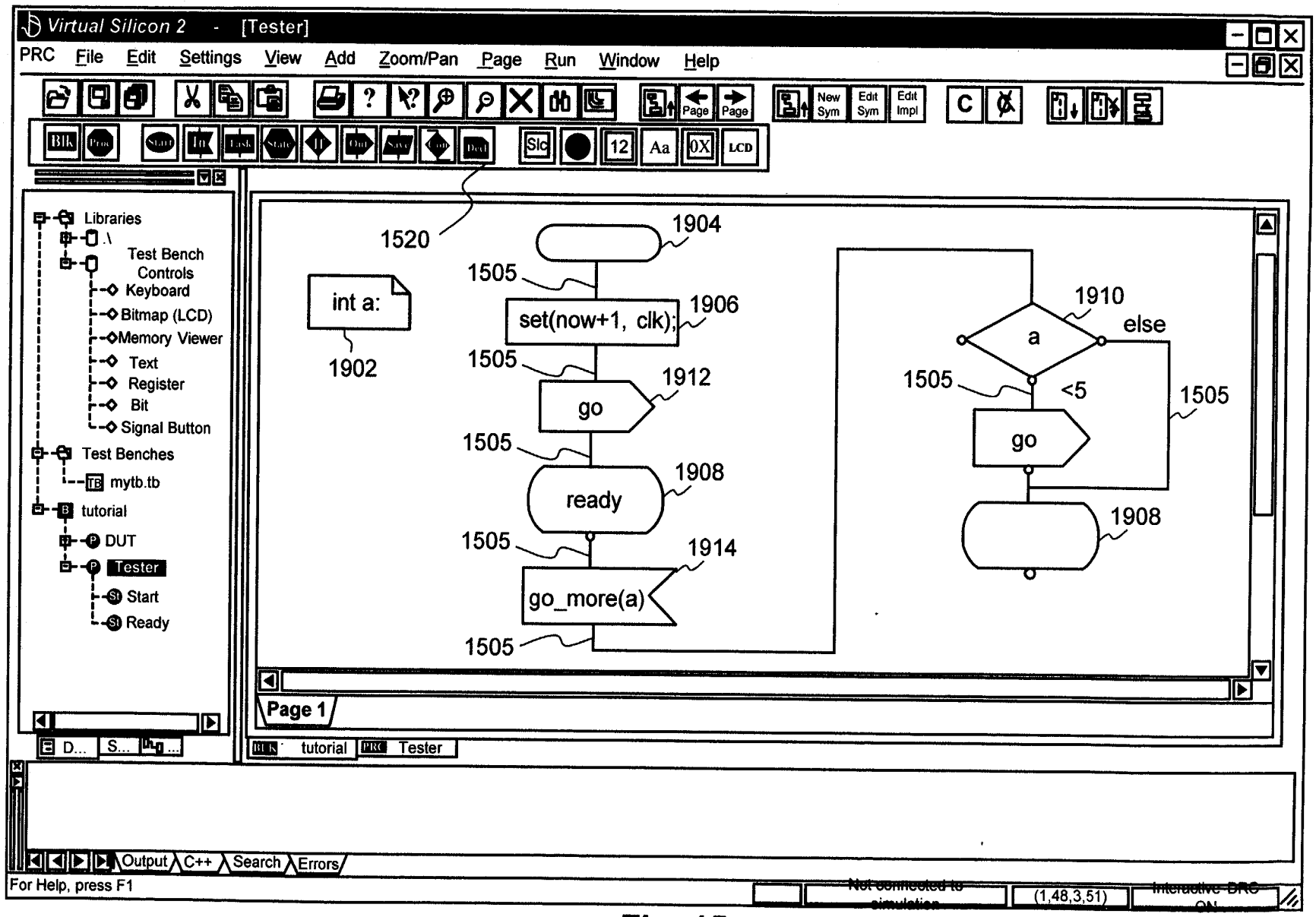

Fig. 15

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
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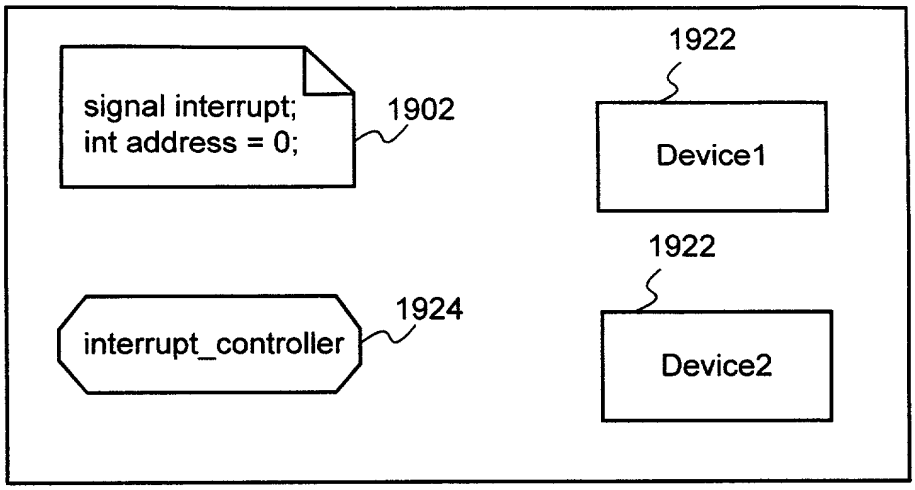


Fig. 16

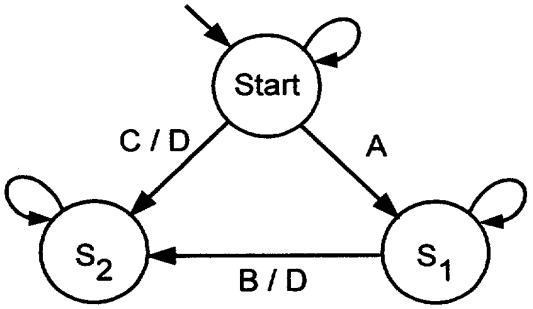


Fig. 17(a)

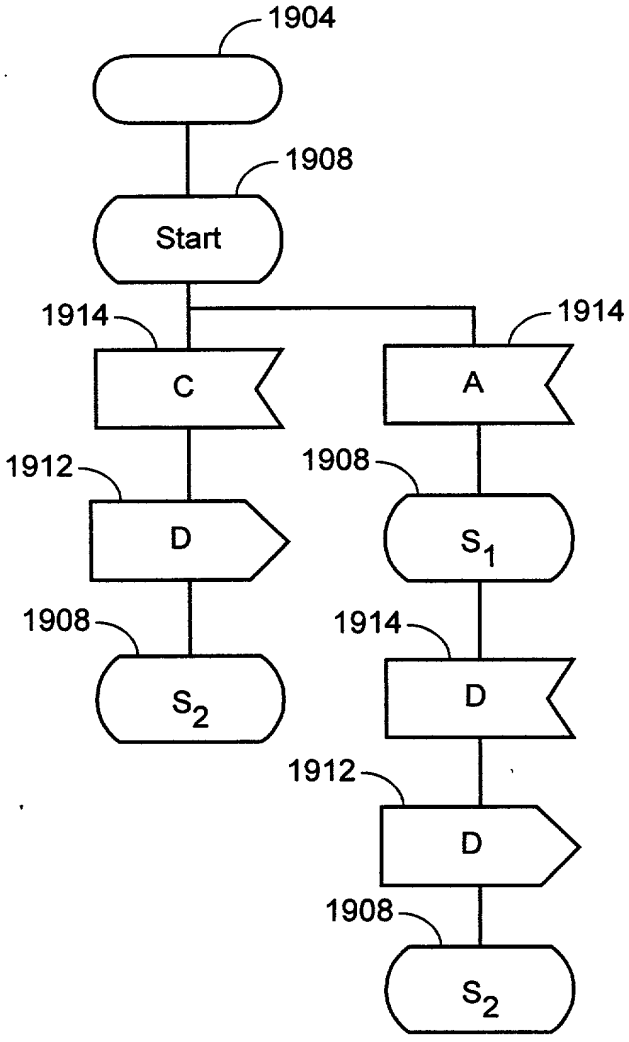


Fig. 17(b)

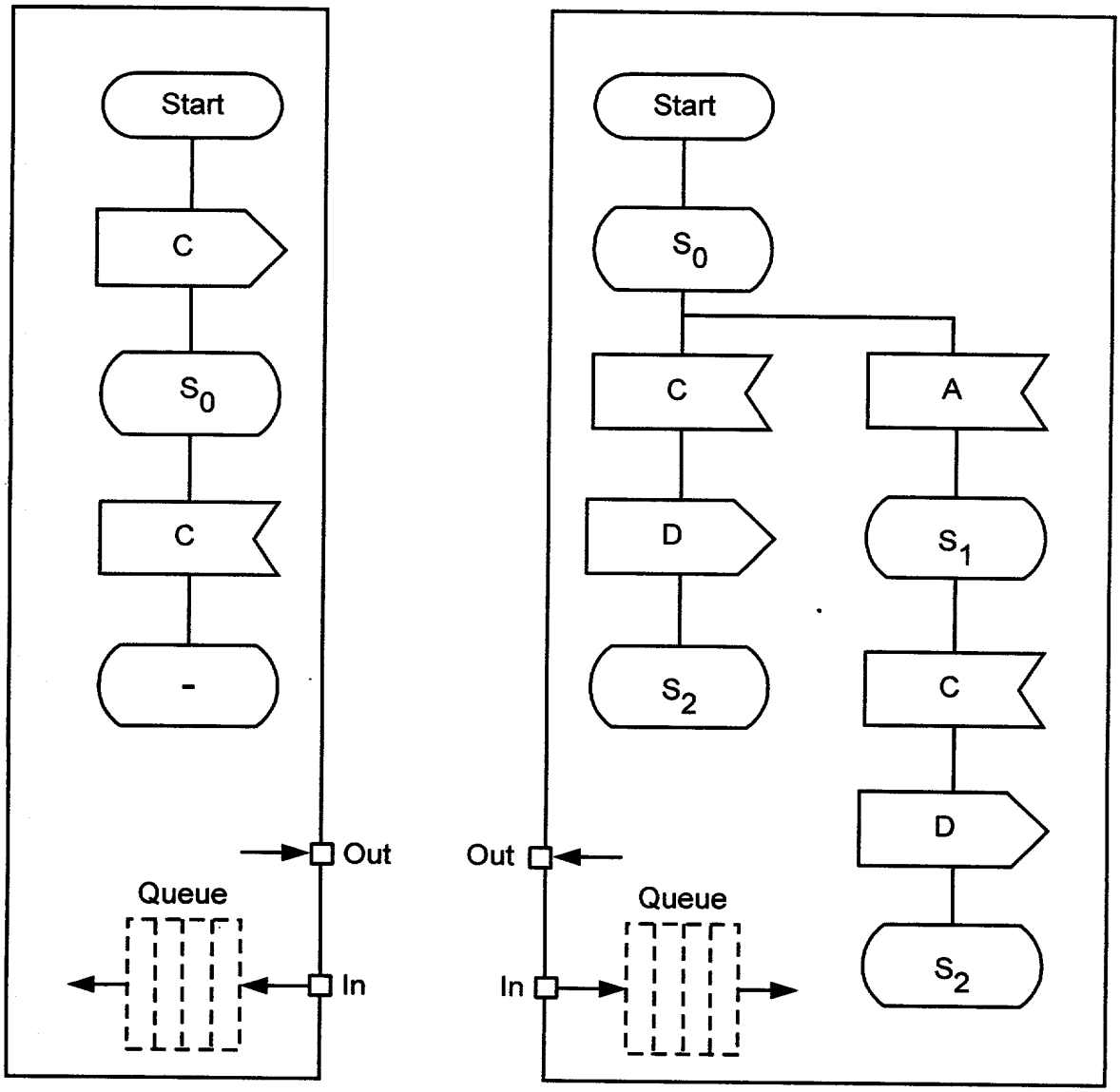


Fig. 18

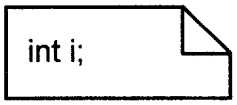
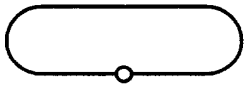
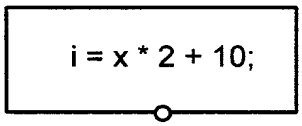
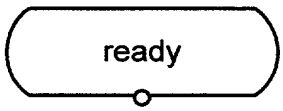
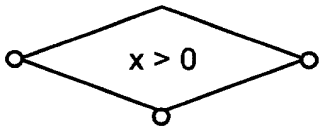
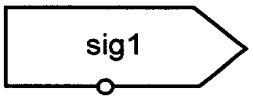
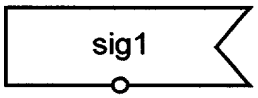
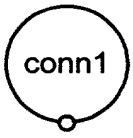
	Name	Graphical Symbol	Description
1902	Declaration		defines local variables and signals.
1904	Start		Starting point of the Finite State Machine execution at initialization time
1906	Task		Execution block, containing ANSI-C statements to be executed
1908	State		Location where FSM waits in until a triggering signal is received.
1910	Decision		Directs execution flow based on the result of expression evaluation inside the decision construct.
1912	Signal-Out		Sending of a communication signal (with an optional payload)
1914	Signal-In		Receiving of a communication signal (with an optional payload)
1916	Connector		Allows to split designs over multiple pages, and connects the control flow between these different pages.

Fig. 19A

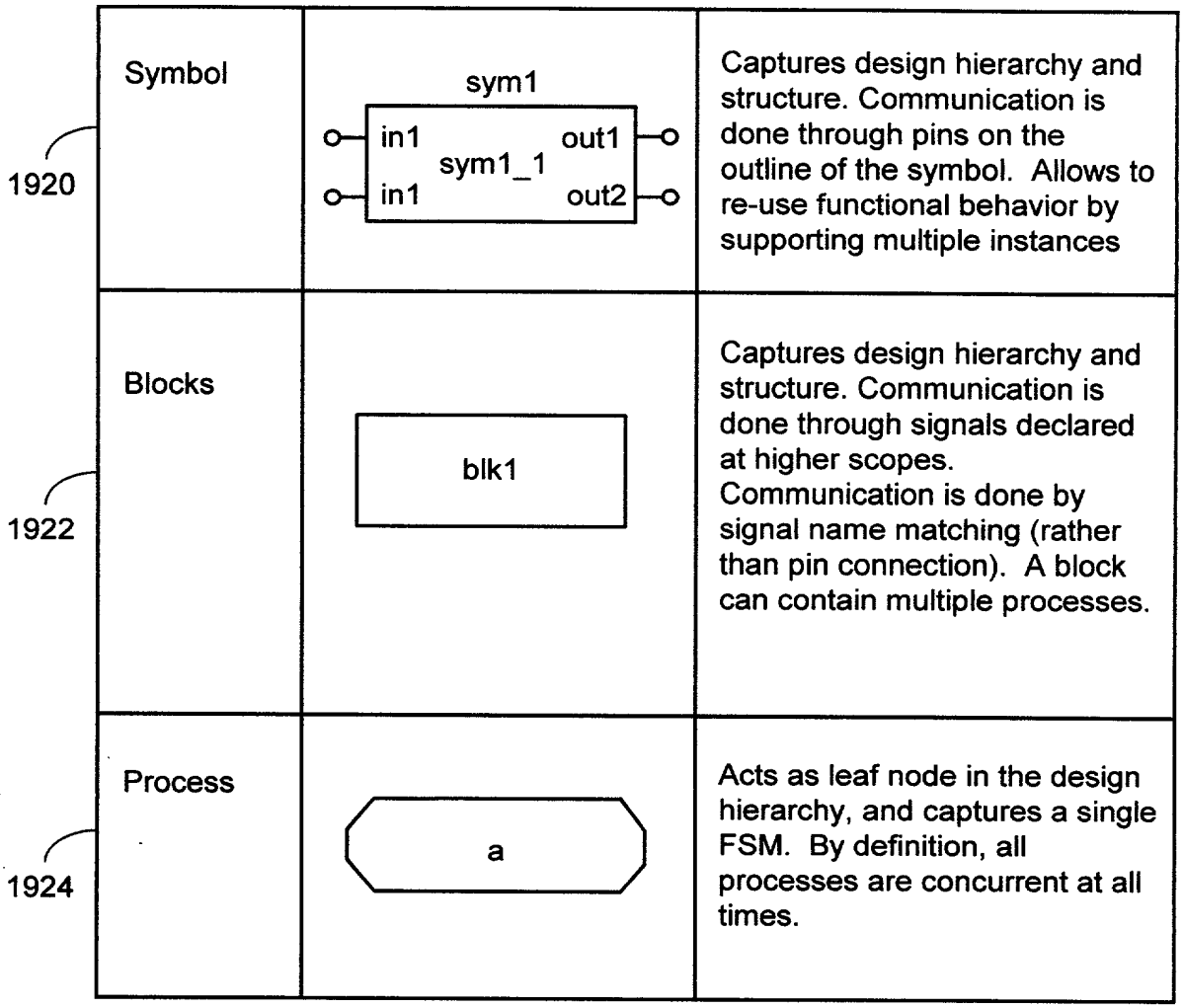

Symbol
1920
sym1
in1
in1
sym1_1
out1
out2
Captures design hierarchy and structure. Communication is done through pins on the outline of the symbol. Allows to re-use functional behavior by supporting multiple instances
Blocks
1922
blk1
Captures design hierarchy and structure. Communication is done through signals declared at higher scopes. Communication is done by signal name matching (rather than pin connection). A block can contain multiple processes.
Process
1924
a
Acts as leaf node in the design hierarchy, and captures a single FSM. By definition, all processes are concurrent at all times.

Fig. 19B

```
// External interface
extern_signal WR(unsigned int, unsigned int,
unsigned int);
extern_signal RD(unsigned int, unsigned int);
extern_signal Write_Ack;
extern_signal Read_Data(unsigned int);
extern_signal CNTINTR(unsigned int);
// Local variables
signal start_clk;
clock clk;
bool clock_started;
unsigned int LIMIT; //write register
VS_int COUNT;
//temp vars
unsigned int data, width, addr;
```

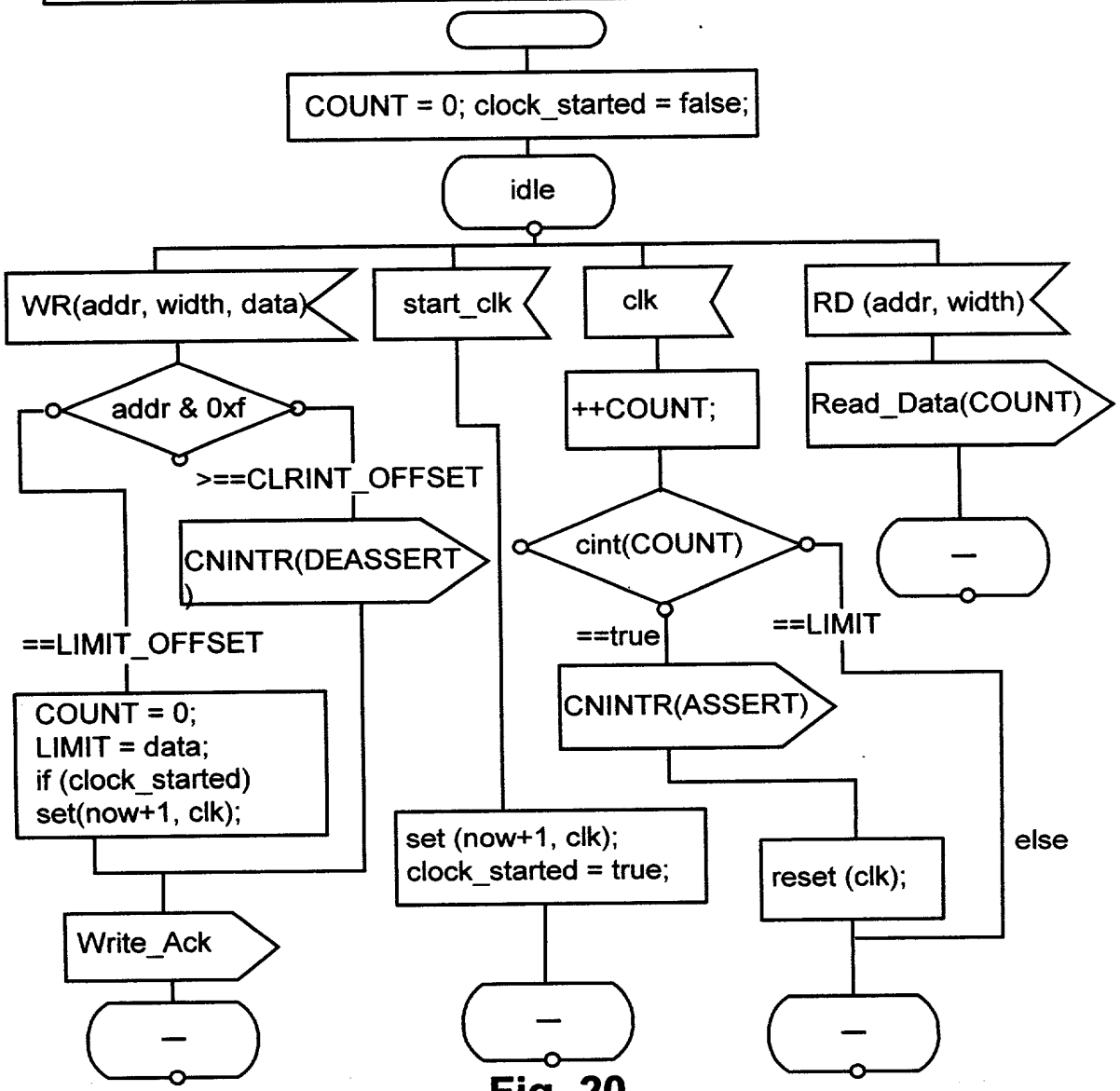


Fig. 20

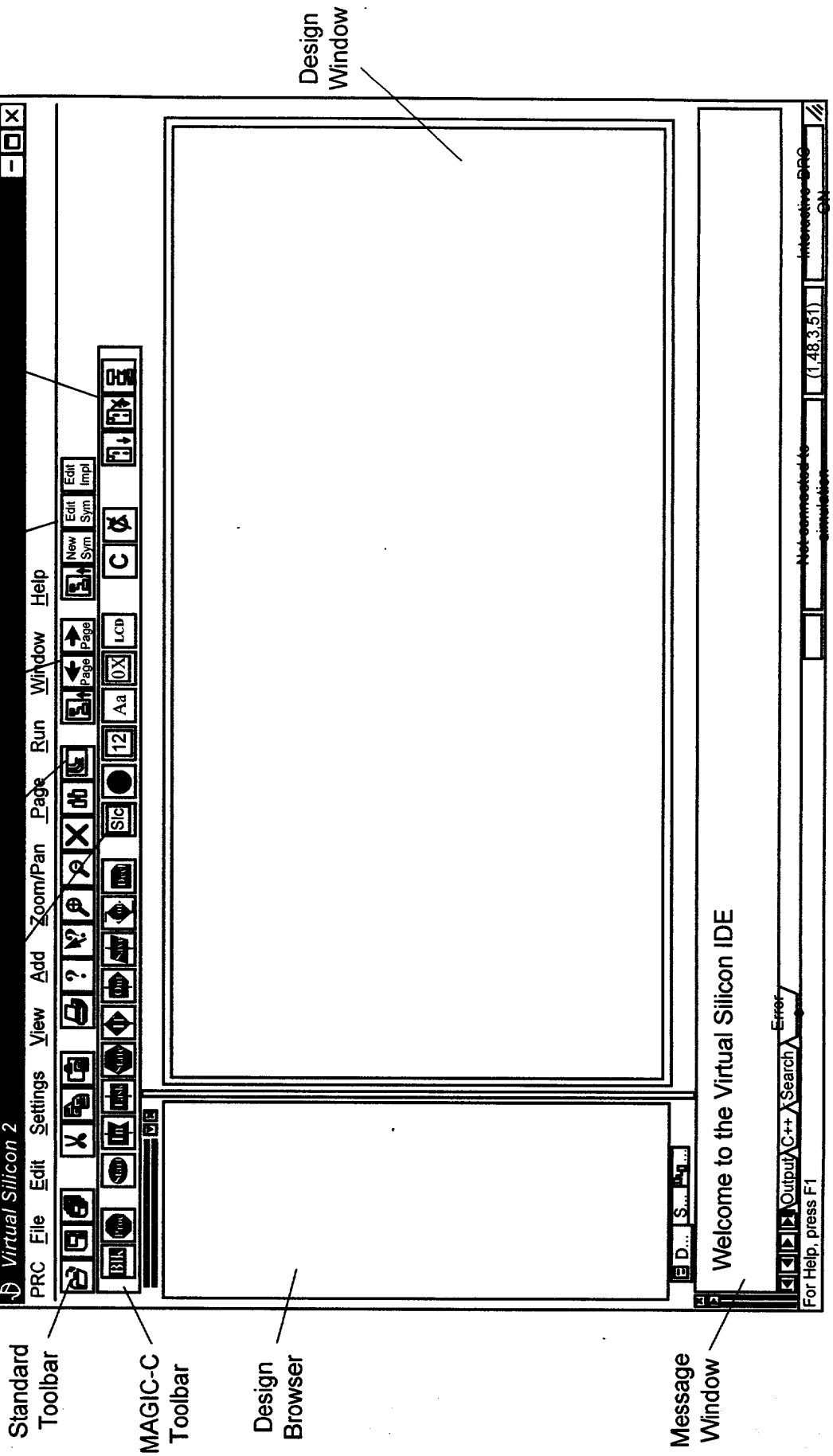
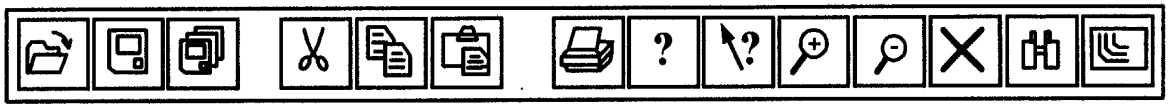
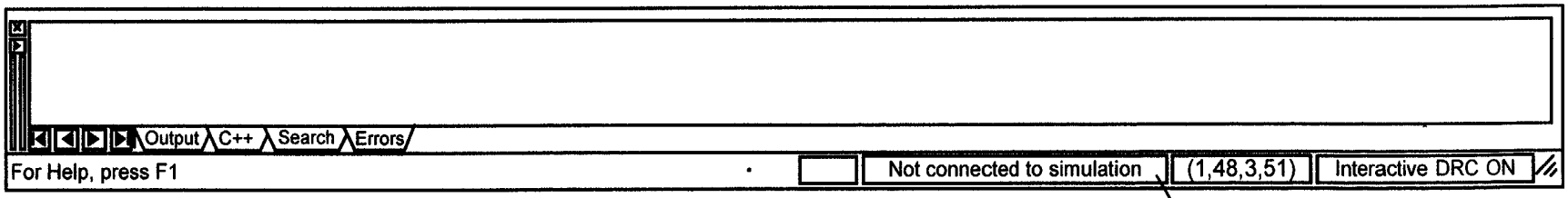

Design Window
Compiler/Debugger Toolbar
Symbol Editor Toolbar
Navigation Toolbar
WaveViewer
Test Bench Builder Toolbar
Standard Toolbar
MAGIC-C Toolbar
Design Browser
Message Window
Virtual Silicon 2
PRC File Edit Settings View Add Zoom/Pan Page Run Window Help
Welcome to the Virtual Silicon IDE
For Help, press F1

Fig. 21



Standard Toolbar

Fig. 22



Message Window, Showing Different Message Tabs, and the Status Bar

Fig. 27

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Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
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Atty. Docket No.: 22178-05012
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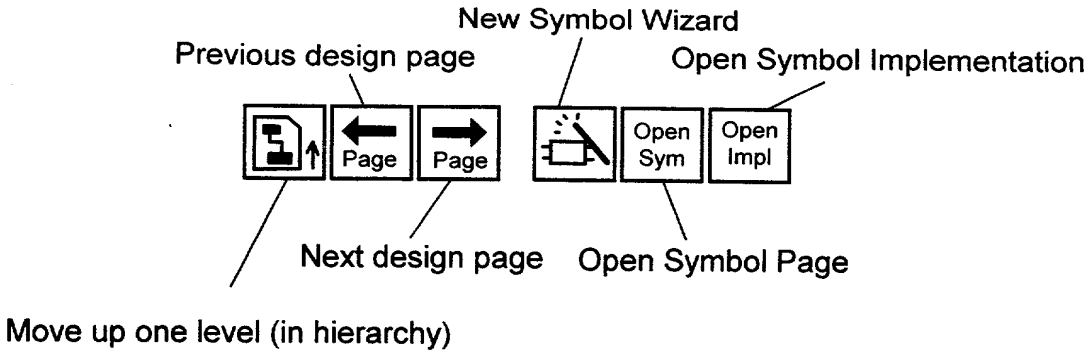

Fig. 23

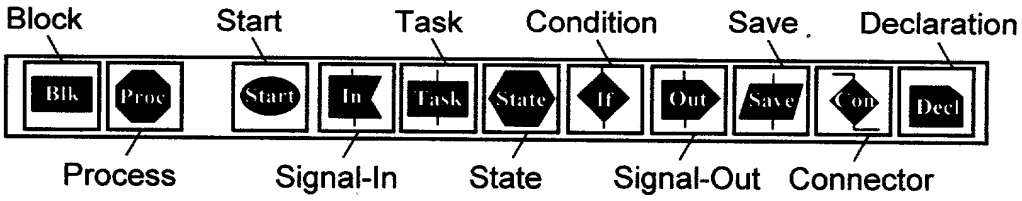

Fig. 24

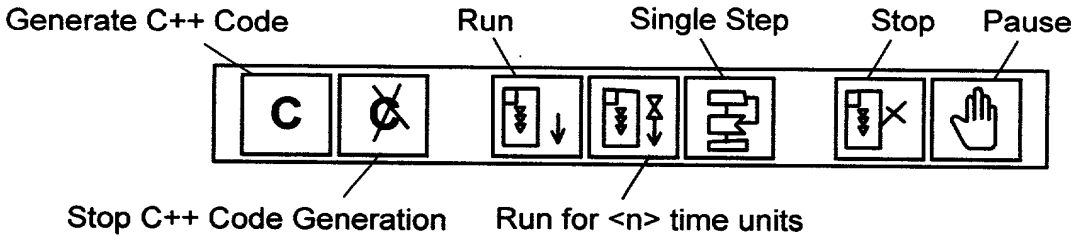

Fig. 25

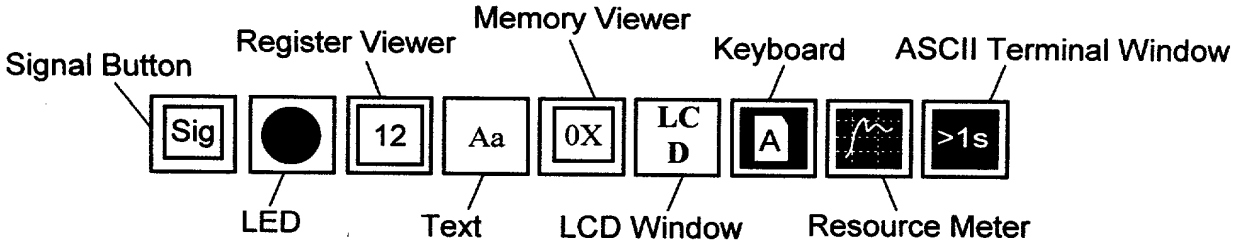

Fig. 26

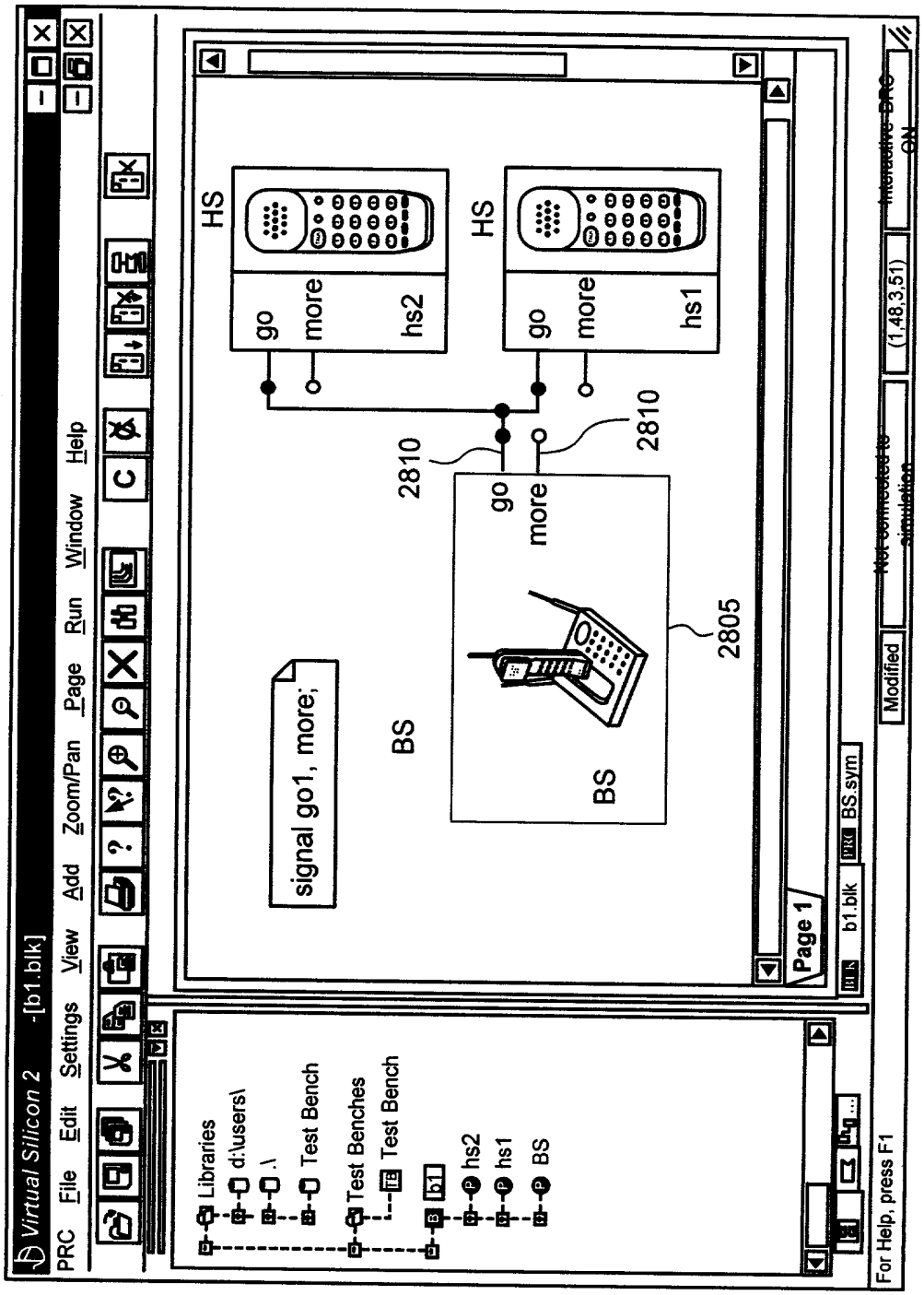
Virtual Silicon 2 -[b1.blk]
PRC File Edit Settings View Add Zoom/Pan Page Run Window Help
Libraries
d:\users\
.\
Test Bench
Test Benches
Test Bench
b1
hs2
hs1
BS
HS
go
more
hs2
HS
go
more
hs1
2810
2810
go
more
BS
2805
signal go1, more;
BS
Page 1
b1.blk
BS.sym
Modified
Not connected to simulation
(1.48,3.51)
Interactive DRC ON
For Help, press F1

Fig. 28

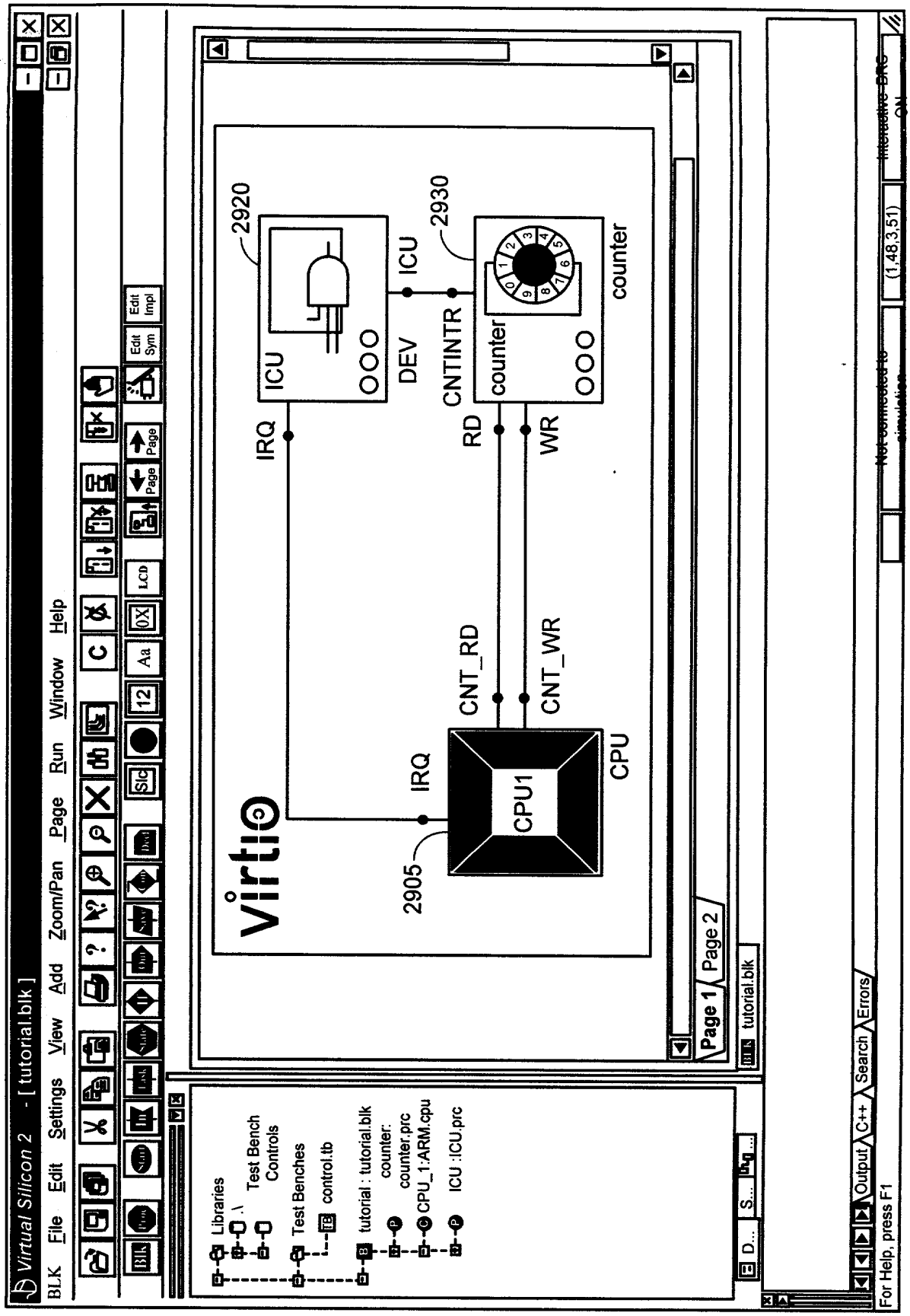
Virtual Silicon 2 - [tutorial.blk]
BLK File Edit Settings View Add Zoom/Pan Page Run Window Help
Libraries
Test Bench Controls
Test Benches
control.tb
tutorial : tutorial.blk
counter: counter.prc
CPU_1:ARM.cpu
ICU :ICU.prc
virtio
2920
ICU
IRQ
DEV
ICU
2930
CNTINTR
counter
RD
WR
counter
2905
IRQ
CNT_RD
CNT_WR
CPU1
CPU
Page 1
Page 2
tutorial.blk
Output
C++
Search
Errors
For Help, press F1
(1,48,3,51)

Fig. 29

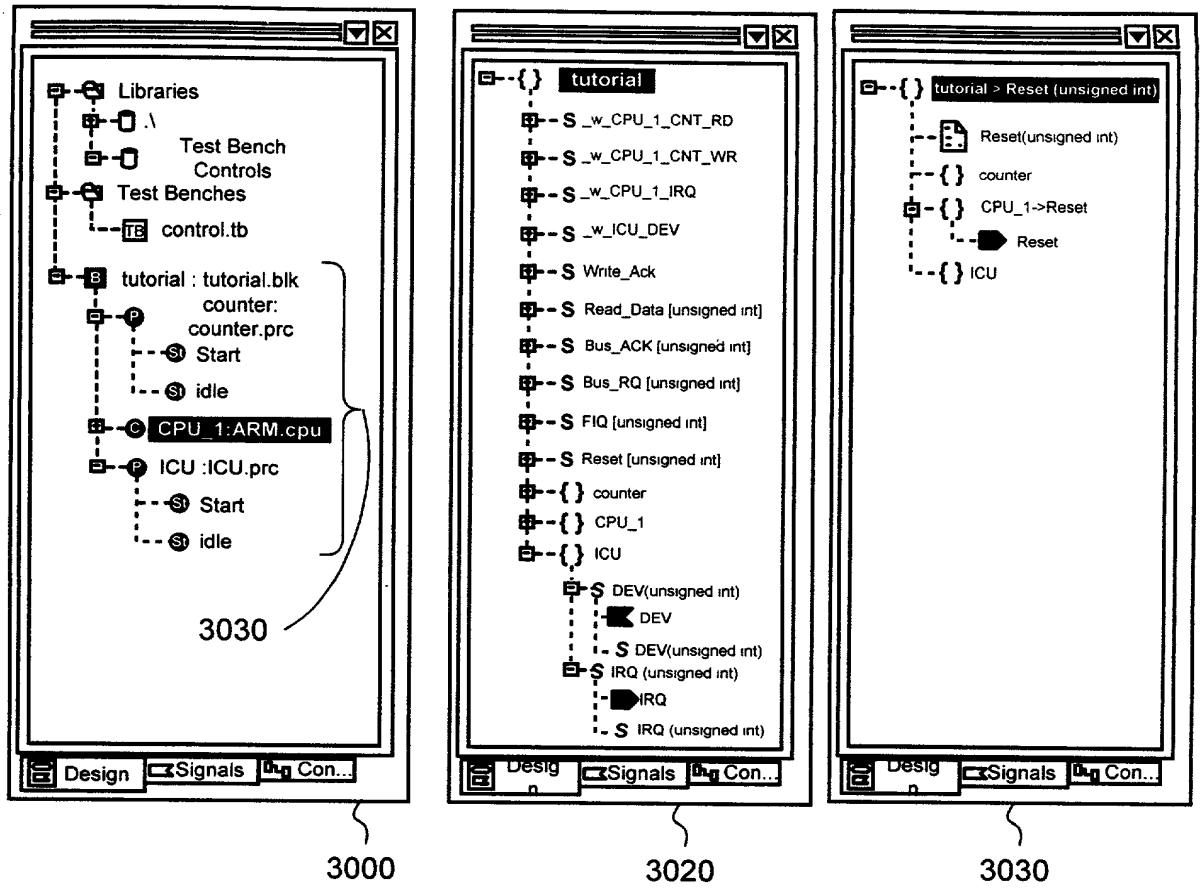
Libraries
.\
Test Bench Controls
Test Benches
control.tb
tutorial : tutorial.blk
counter: counter.prc
Start
idle
CPU_1:ARM.cpu
ICU :ICU.prc
Start
idle
3030
Design
Signals
Con...
3000
tutorial
_w_CPU_1_CNT_RD
_w_CPU_1_CNT_WR
_w_CPU_1_IRQ
_w_ICU_DEV
Write_Ack
Read_Data [unsigned int]
Bus_ACK [unsigned int]
Bus_RQ [unsigned int]
FIQ [unsigned int]
Reset [unsigned int]
counter
CPU_1
ICU
DEV(unsigned int)
DEV
DEV(unsigned int)
IRQ (unsigned int)
IRQ
IRQ (unsigned int)
Signals
Con...
3020
tutorial > Reset (unsigned int)
Reset(unsigned int)
counter
CPU_1->Reset
Reset
ICU
Signals
Con...
3030

Fig. 30

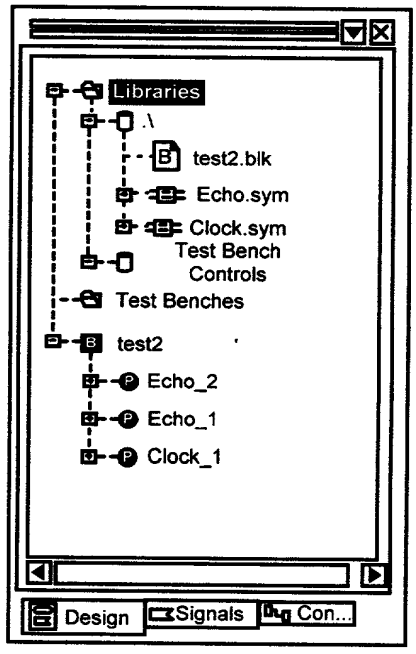
Libraries
.\
test2.blk
Echo.sym
Clock.sym
Test Bench Controls
Test Benches
test2
Echo_2
Echo_1
Clock_1
Design
Signals
Con...

Fig. 31

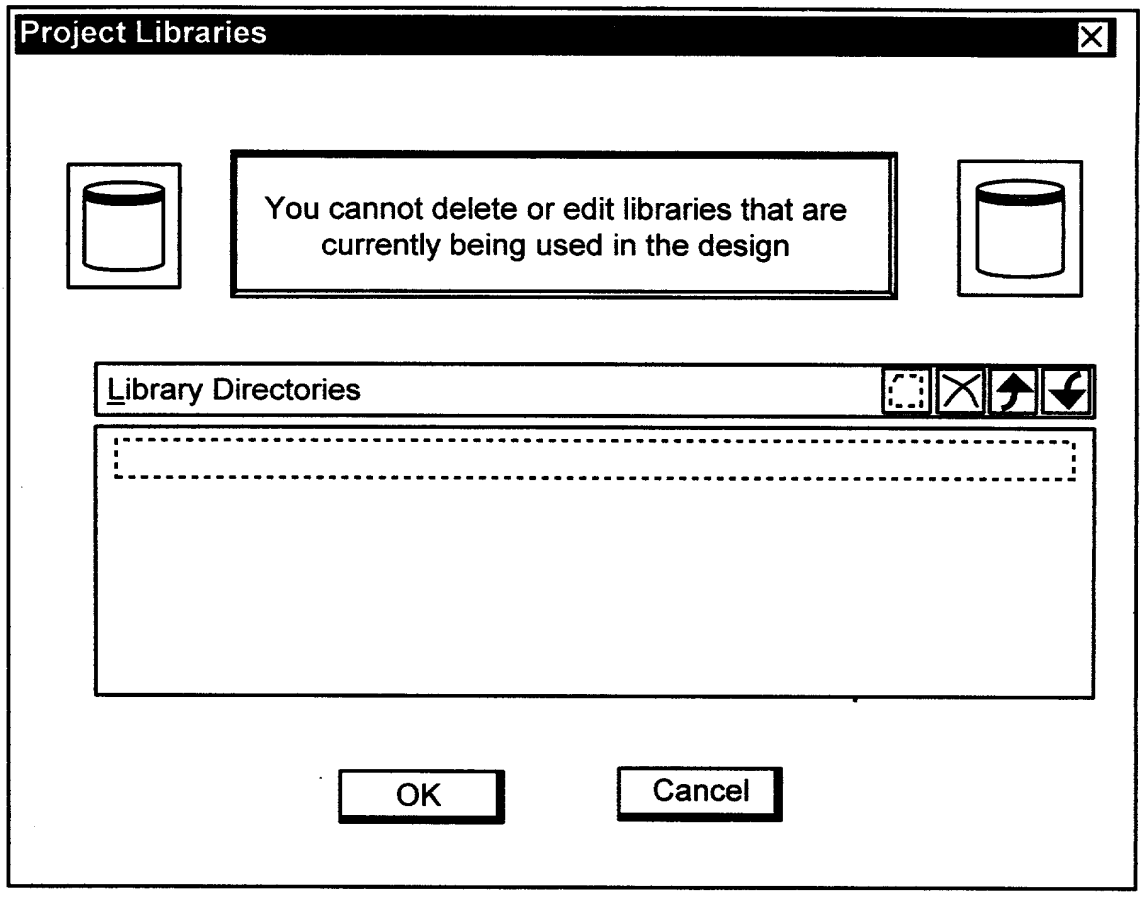
Project Libraries
You cannot delete or edit libraries that are currently being used in the design
Library Directories
OK
Cancel

Fig. 32

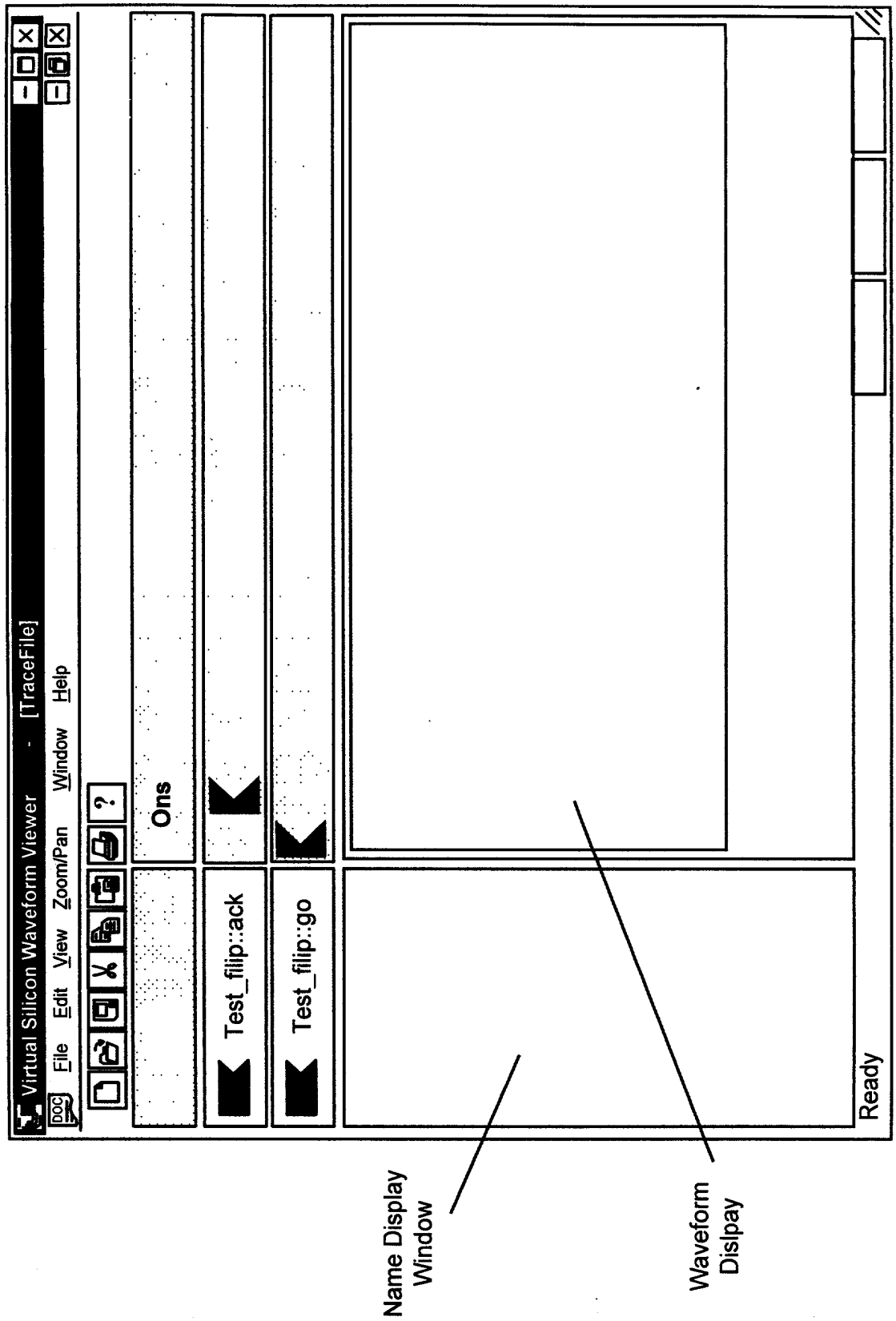
Virtual Silicon Waveform Viewer - [TraceFile]
File Edit View Zoom/Pan Window Help
Ons
Test_filip::ack
Test_filip::go
Ready
Name Display Window
Waveform Dislpay

Fig. 33A

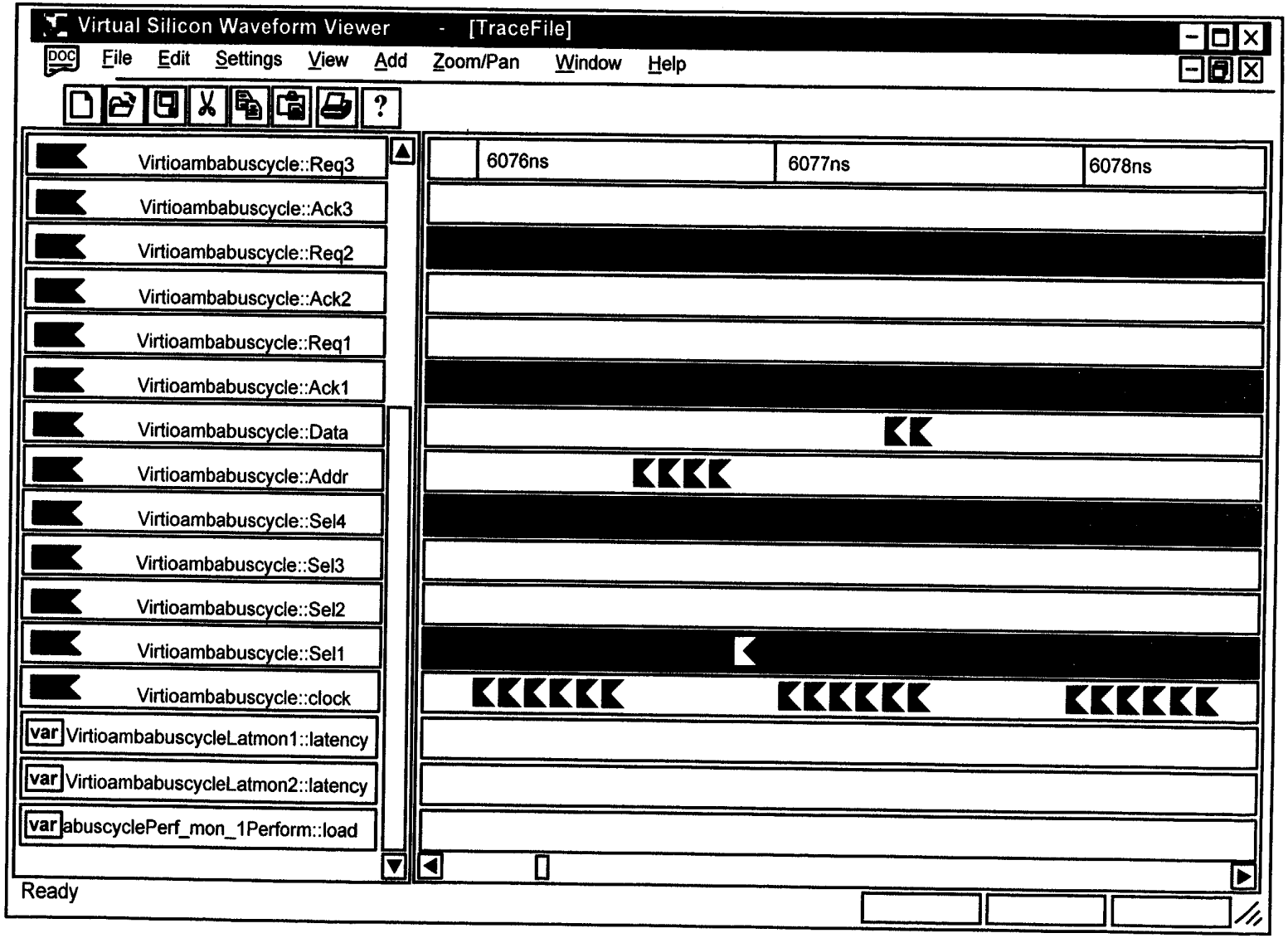
Virtual Silicon Waveform Viewer - [TraceFile]
File Edit Settings View Add Zoom/Pan Window Help
Virtioambabuscycle::Req3
Virtioambabuscycle::Ack3
Virtioambabuscycle::Req2
Virtioambabuscycle::Ack2
Virtioambabuscycle::Req1
Virtioambabuscycle::Ack1
Virtioambabuscycle::Data
Virtioambabuscycle::Addr
Virtioambabuscycle::Sel4
Virtioambabuscycle::Sel3
Virtioambabuscycle::Sel2
Virtioambabuscycle::Sel1
Virtioambabuscycle::clock
var VirtioambabuscycleLatmon1::latency
var VirtioambabuscycleLatmon2::latency
var abuscyclePerf_mon_1Perform::load
6076ns
6077ns
6078ns
Ready

Fig. 33B

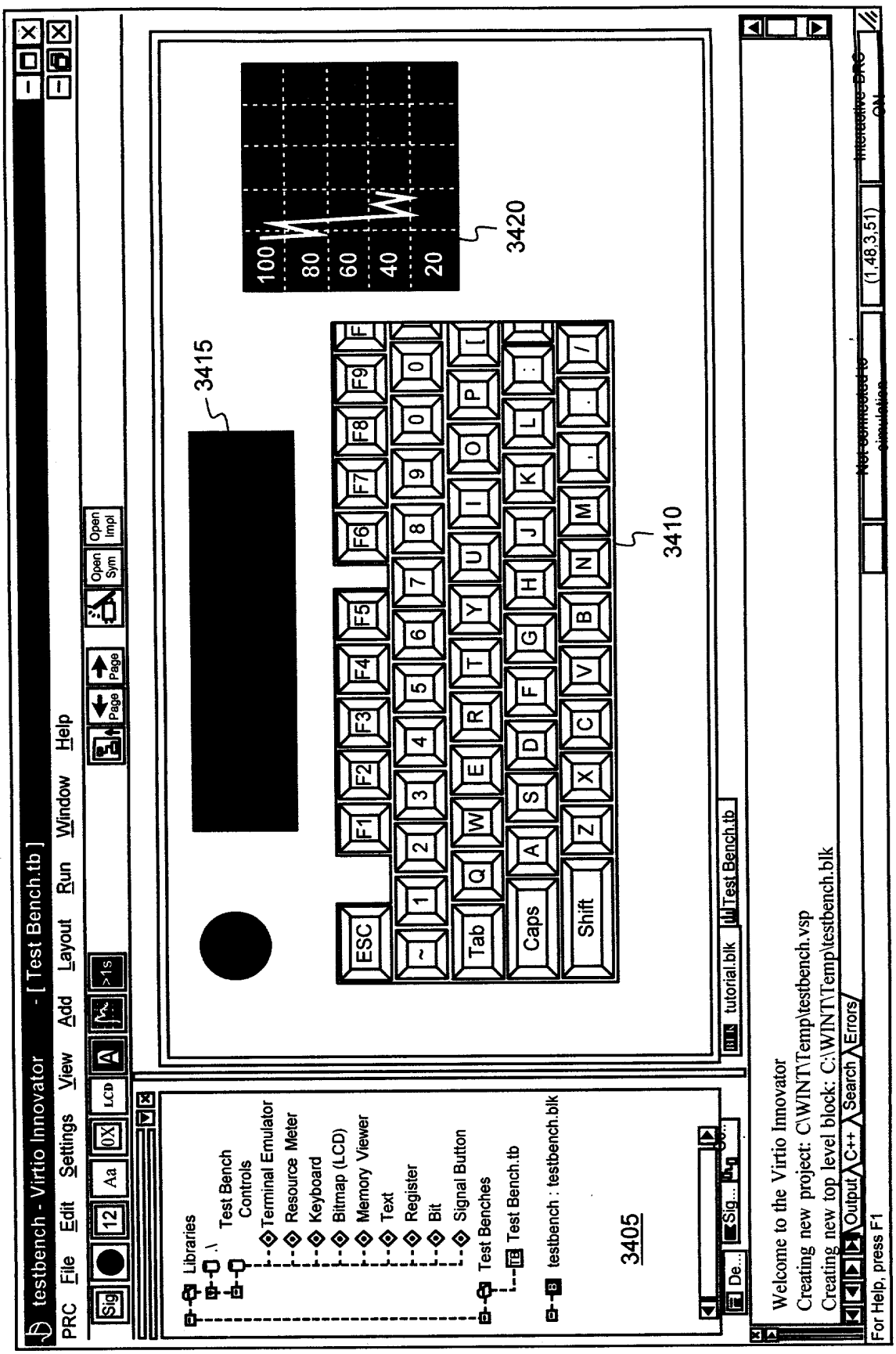
testbench - Virtio Innovator - [Test Bench.tb]
PRC File Edit Settings View Add Layout Run Window Help
Libraries
Test Bench Controls
Terminal Emulator
Resource Meter
Keyboard
Bitmap (LCD)
Memory Viewer
Text
Register
Bit
Signal Button
Test Benches
Test Bench.tb
testbench : testbench.blk
3405
3410
3415
3420
100
80
60
40
20
Welcome to the Virtio Innovator
Creating new project: C\WINT\Temp\testbench.vsp
Creating new top level block: C:\WINT\Temp\testbench.blk
For Help, press F1

Fig. 34A

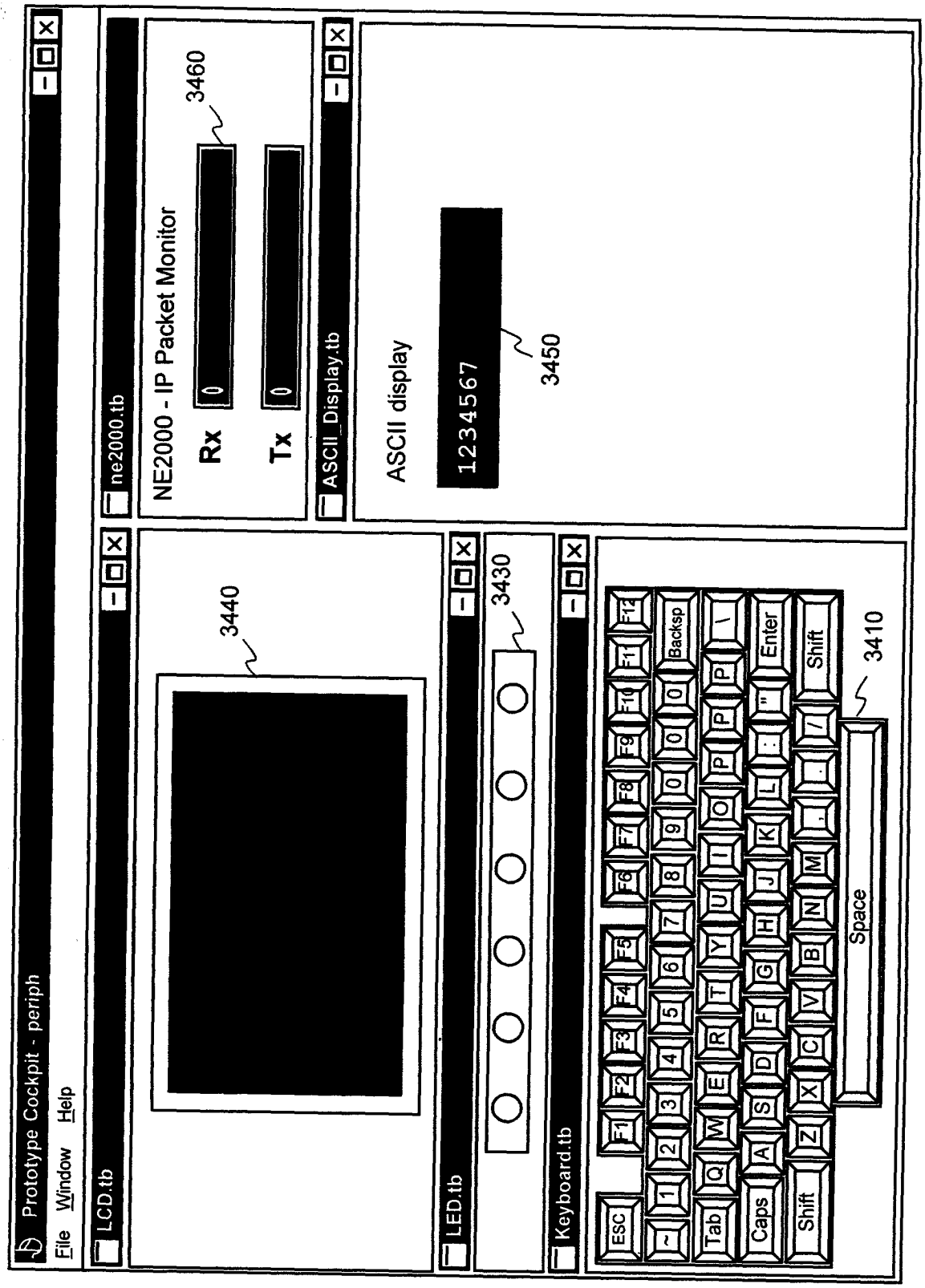
Prototype Cockpit - periph
File Window Help
LCD.tb
3440
LED.tb
3430
ne2000.tb
NE2000 - IP Packet Monitor
3460
Rx
Tx
0
0
ASCII_Display.tb
ASCII display
1234567
3450
Keyboard.tb
3410
ESC
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
~
1
2
3
4
5
6
7
8
9
0
Backsp
Tab
Q
W
E
R
T
Y
U
I
O
P
Caps
A
S
D
F
G
H
J
K
L
Enter
Shift
Z
X
C
V
B
N
M
Space

Fig. 34B

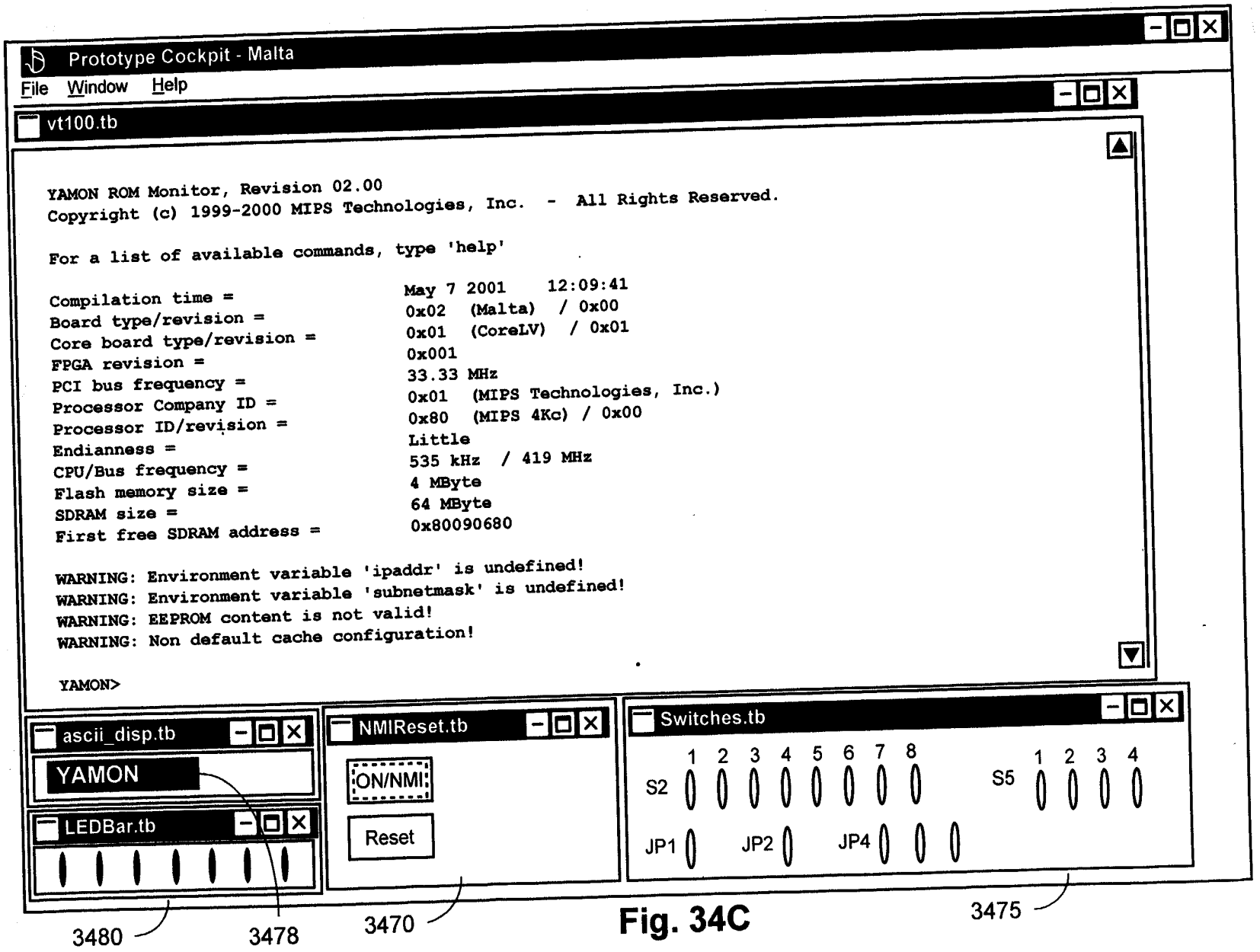
Prototype Cockpit - Malta
File Window Help
vt100.tb
YAMON ROM Monitor, Revision 02.00
Copyright (c) 1999-2000 MIPS Technologies, Inc. - All Rights Reserved.
For a list of available commands, type 'help'
Compilation time = May 7 2001 12:09:41
Board type/revision = 0x02 (Malta) / 0x00
Core board type/revision = 0x01 (CoreLV) / 0x01
FPGA revision = 0x001
PCI bus frequency = 33.33 MHz
Processor Company ID = 0x01 (MIPS Technologies, Inc.)
Processor ID/revision = 0x80 (MIPS 4Kc) / 0x00
Endianness = Little
CPU/Bus frequency = 535 kHz / 419 MHz
Flash memory size = 4 MByte
SDRAM size = 64 MByte
First free SDRAM address = 0x80090680
WARNING: Environment variable 'ipaddr' is undefined!
WARNING: Environment variable 'subnetmask' is undefined!
WARNING: EEPROM content is not valid!
WARNING: Non default cache configuration!
YAMON>
ascii_disp.tb
YAMON
LEDBar.tb
NMIReset.tb
ON/NMI
Reset
Switches.tb
S2
1 2 3 4 5 6 7 8
S5
1 2 3 4
JP1
JP2
JP4
3480
3478
3470
3475

Fig. 34C

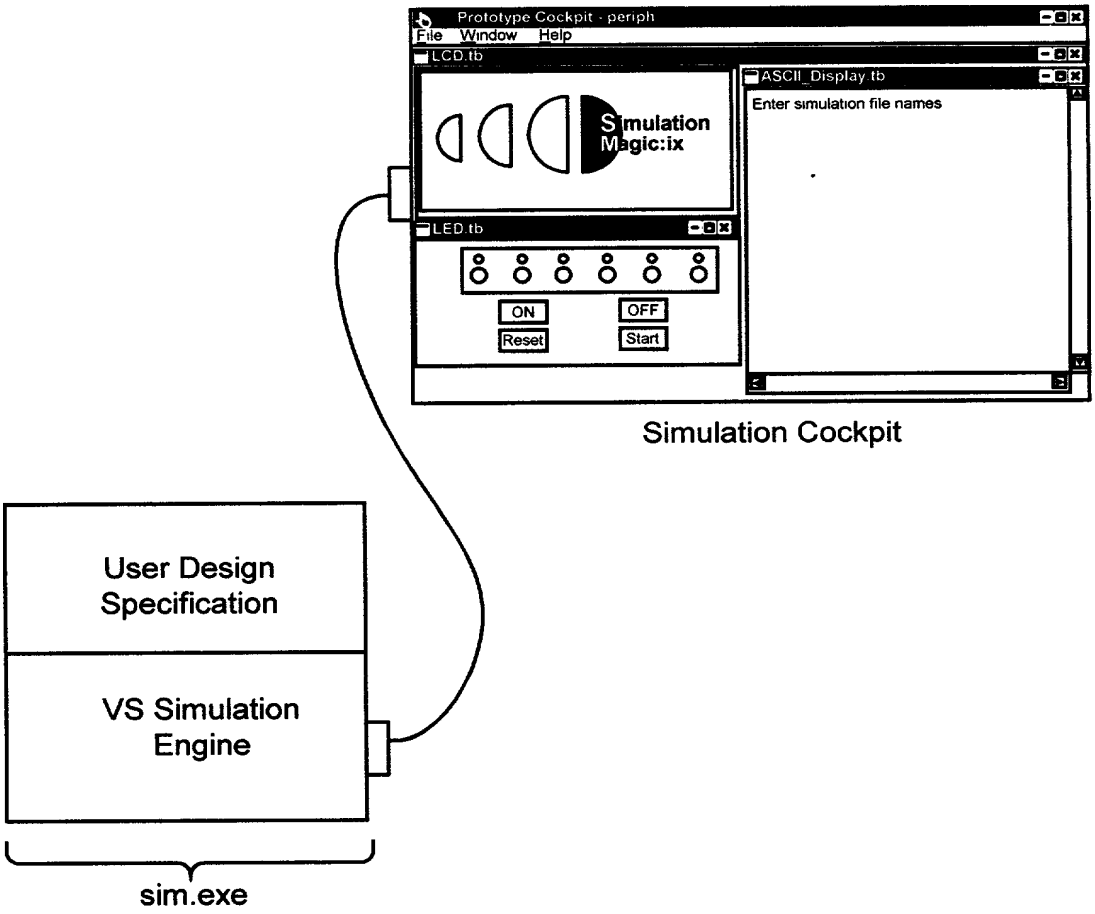
Prototype Cockpit - periph
File Window Help
LCD.tb
Simulation Magic:ix
ASCII_Display.tb
Enter simulation file names
LED.tb
ON
OFF
Reset
Start
Simulation Cockpit
User Design Specification
VS Simulation Engine
sim.exe

Fig. 35

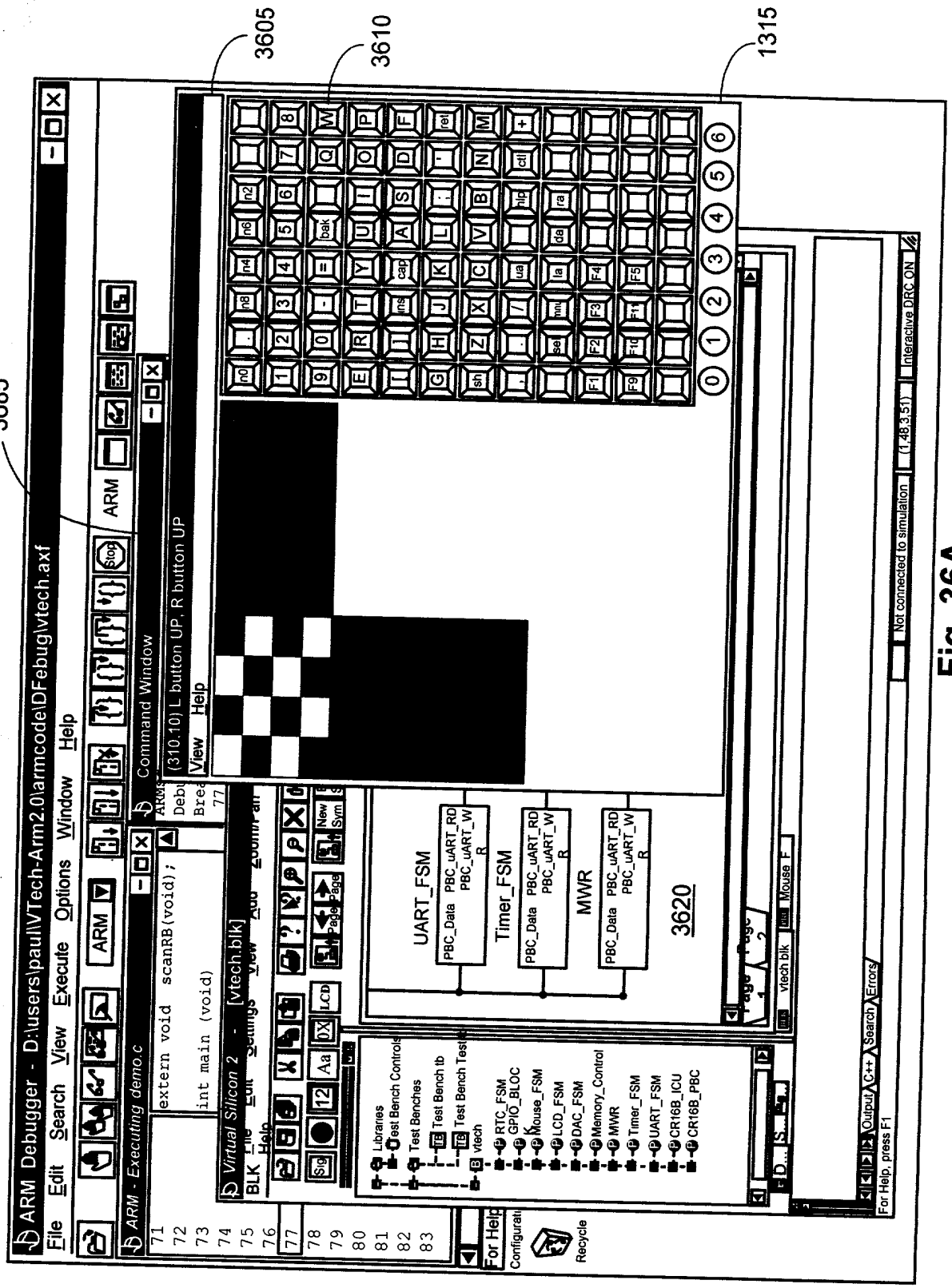
3685
3605
3610
1315
3620
ARM Debugger - D:\users\paul\VTech-Arm2.0\armcode\DFebug\vtech.axf
File Edit Search View Execute Options Window Help
ARM - Executing demo.c
Command Window
Virtual Silicon 2 - [vtech.blk]
(310,10) L button UP, R button UP
View Help
UART_FSM
Timer_FSM
MWR
PBC_Data
PBC_uART_RD
PBC_uART_WR
Not connected to simulation
Interactive DRC ON
For Help, press F1

Fig. 36A

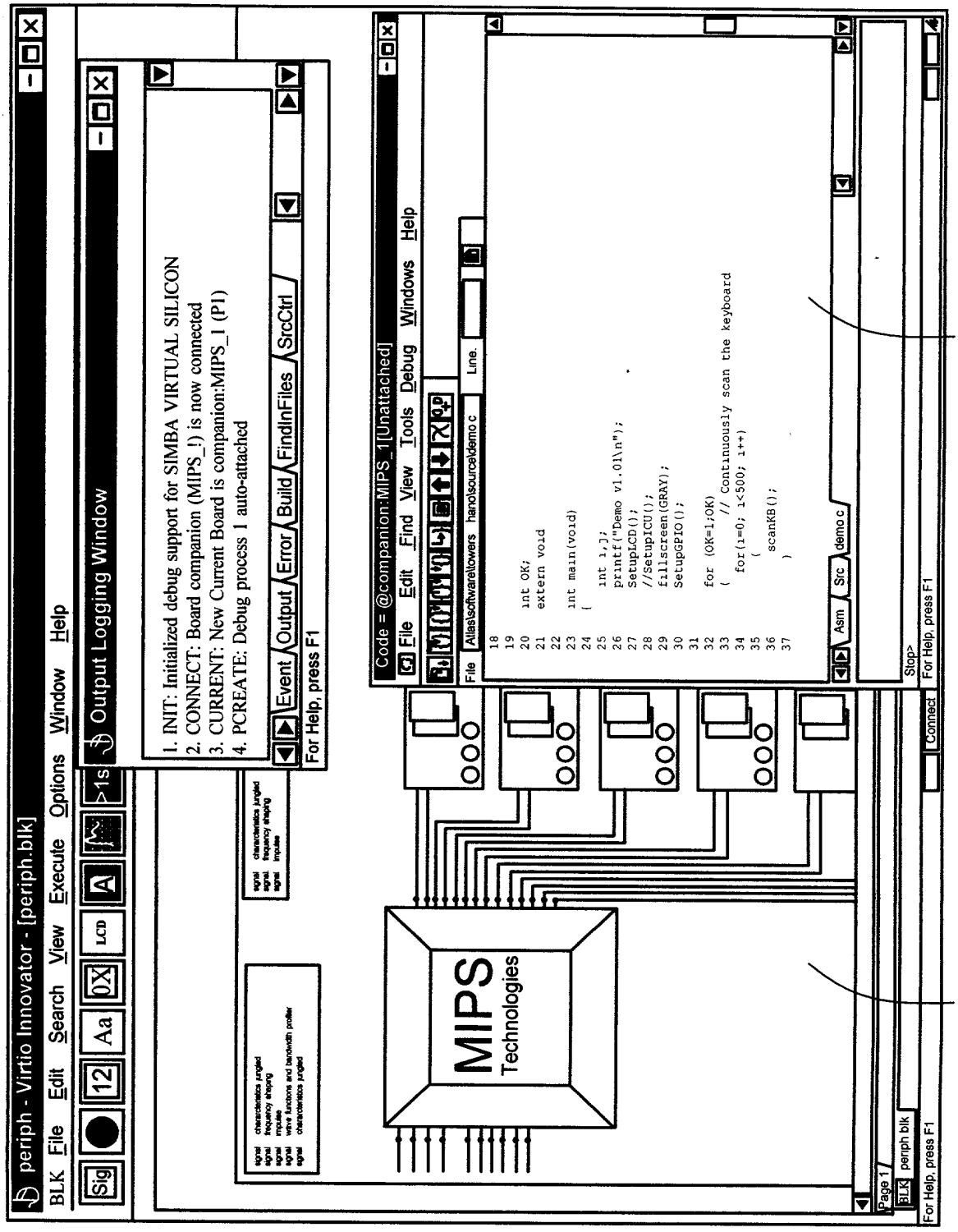
periph - Virtio Innovator - [periph.blk]
BLK File Edit Search View Execute Options Window Help
Output Logging Window
1. INIT: Initialized debug support for SIMBA VIRTUAL SILICON
2. CONNECT: Board companion (MIPS_1) is now connected
3. CURRENT: New Current Board is companion:MIPS_1 (P1)
4. PCREATE: Debug process 1 auto-attached
Event Output Error Build FindInFiles SrcCtrl
For Help, press F1
Code = @companion:MIPS_1[Unattached]
File Edit Find View Tools Debug Windows Help
Asm Src demo.c
Stop>
For Help, press F1
Connect
periph.blk
Page 1
MIPS Technologies
3620
3685

Fig. 36B

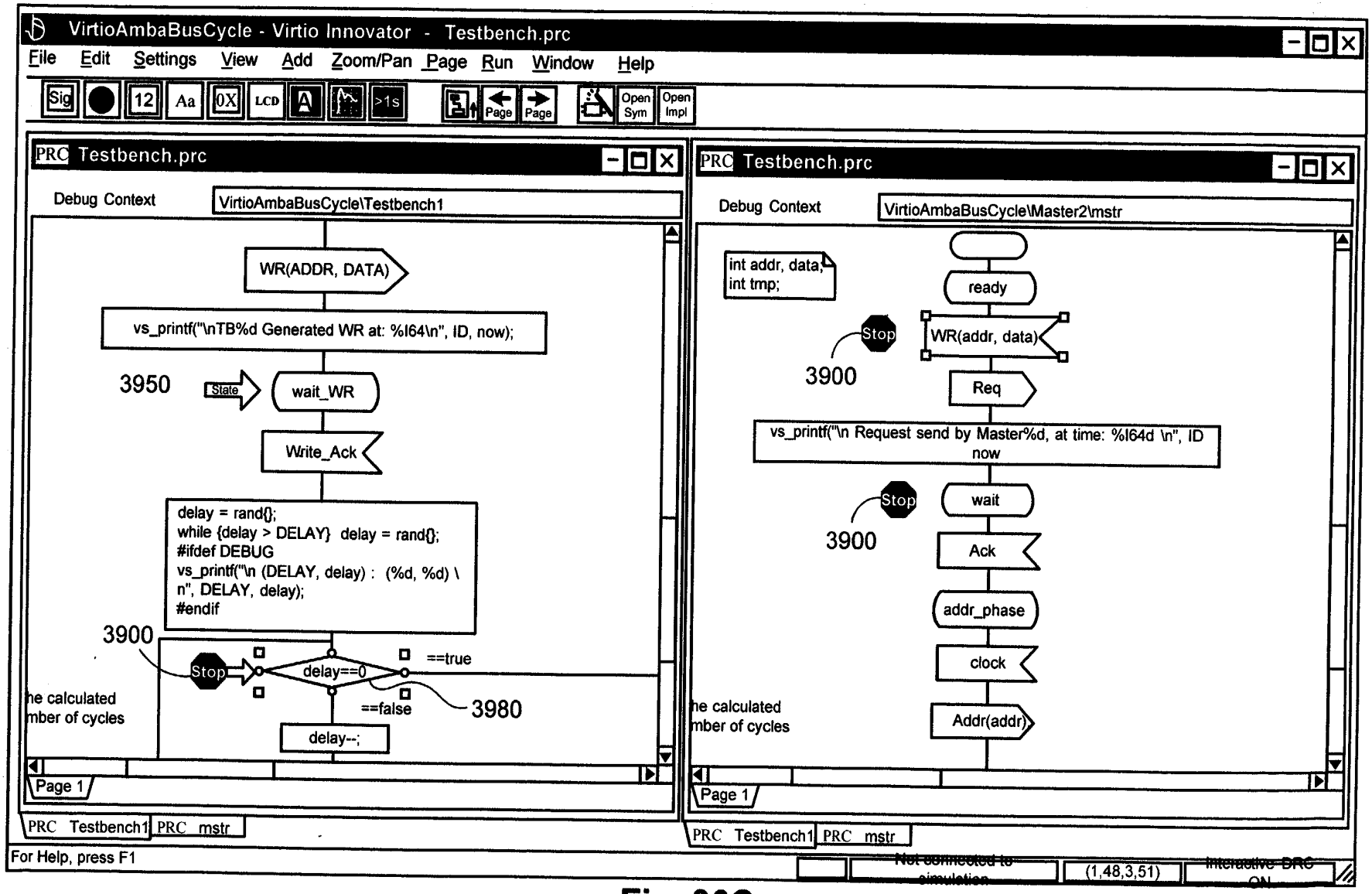
VirtioAmbaBusCycle - Virtio Innovator - Testbench.prc
File Edit Settings View Add Zoom/Pan Page Run Window Help
Sig 12 Aa 0X LCD >1s Page Page Open Sym Open Impl
PRC Testbench.prc
Debug Context
VirtioAmbaBusCycle\Testbench1
WR(ADDR, DATA)
vs_printf("\nTB%d Generated WR at: %l64\n", ID, now);
3950
State
wait_WR
Write_Ack
delay = rand{};
while {delay > DELAY} delay = rand{};
#ifdef DEBUG
vs_printf("\n (DELAY, delay) : (%d, %d) \ n", DELAY, delay);
#endif
3900
Stop
delay==0
==true
==false
3980
delay--;
he calculated
mber of cycles
Page 1
PRC Testbench1
PRC mstr
PRC Testbench.prc
Debug Context
VirtioAmbaBusCycle\Master2\mstr
int addr, data;
int tmp;
ready
Stop
WR(addr, data)
3900
Req
vs_printf("\n Request send by Master%d, at time: %l64d \n", ID now
Stop
wait
3900
Ack
addr_phase
clock
Addr(addr)
he calculated
mber of cycles
Page 1
PRC Testbench1
PRC mstr
For Help, press F1
(1,48,3,51)

Fig. 36C

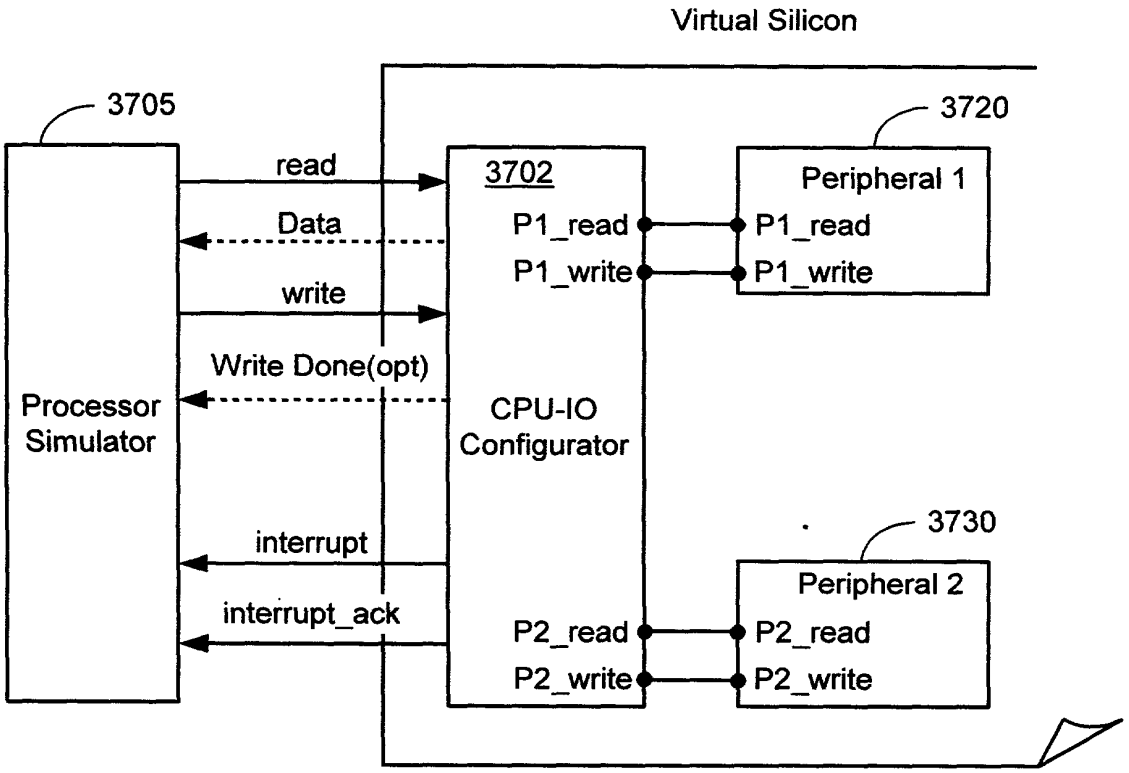
Virtual Silicon
3705
3720
read
3702
Peripheral 1
Data
P1_read
P1_read
P1_write
P1_write
write
Write Done(opt)
Processor Simulator
CPU-IO Configurator
3730
interrupt
Peripheral 2
interrupt_ack
P2_read
P2_read
P2_write
P2_write

Fig. 37

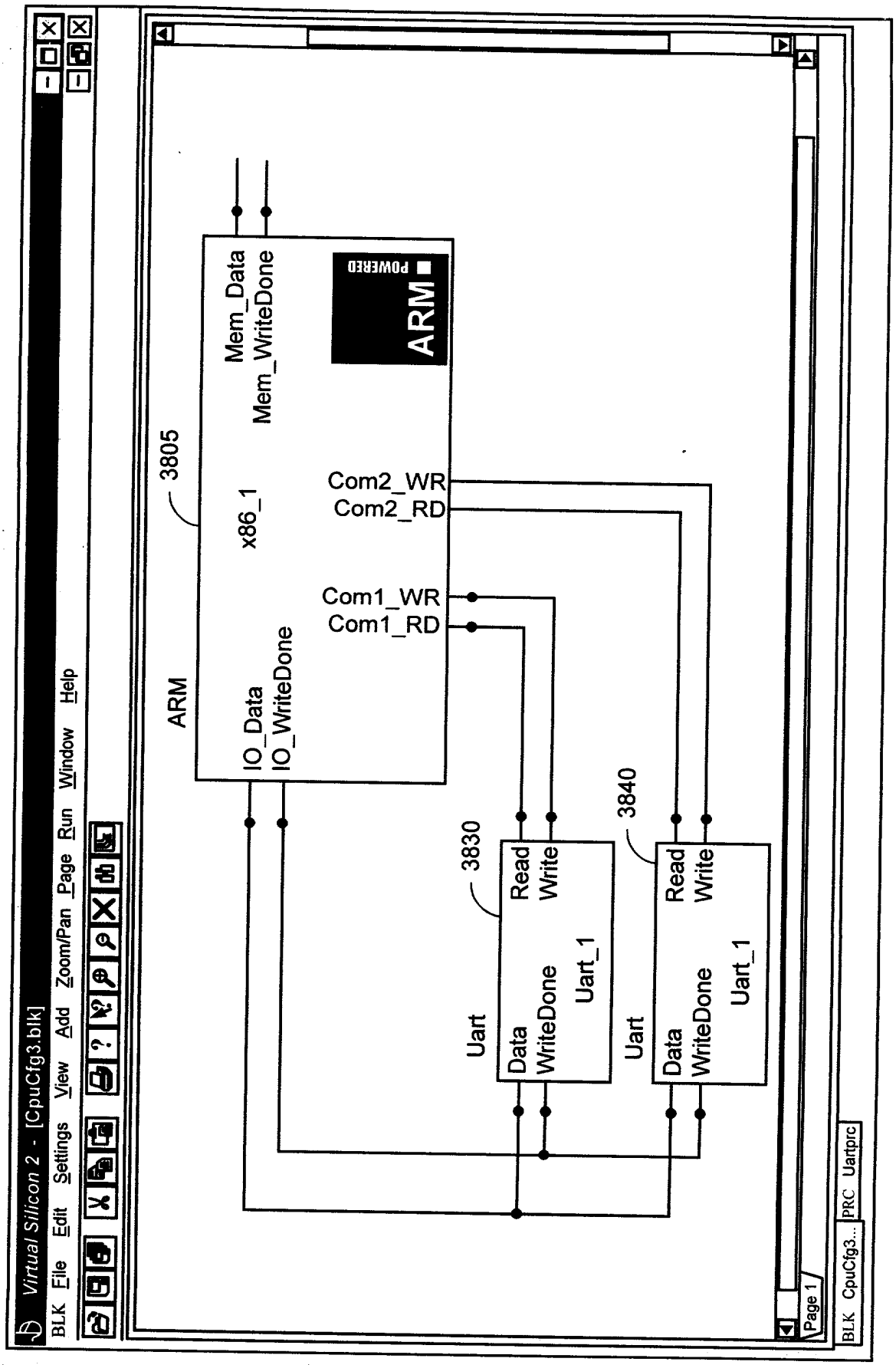
Virtual Silicon 2 - [CpuCfg3.blk]
BLK File Edit Settings View Add Zoom/Pan Page Run Window Help
POWERED
ARM
Mem_Data
Mem_WriteDone
3805
x86_1
ARM
IO_Data
IO_WriteDone
Com2_WR
Com2_RD
Com1_WR
Com1_RD
3830
Read
Write
Uart
Data
WriteDone
Uart_1
3840
Read
Write
Uart
Data
WriteDone
Uart_1
Page 1
BLK CpuCfg3... PRC Uartprc

Fig. 38

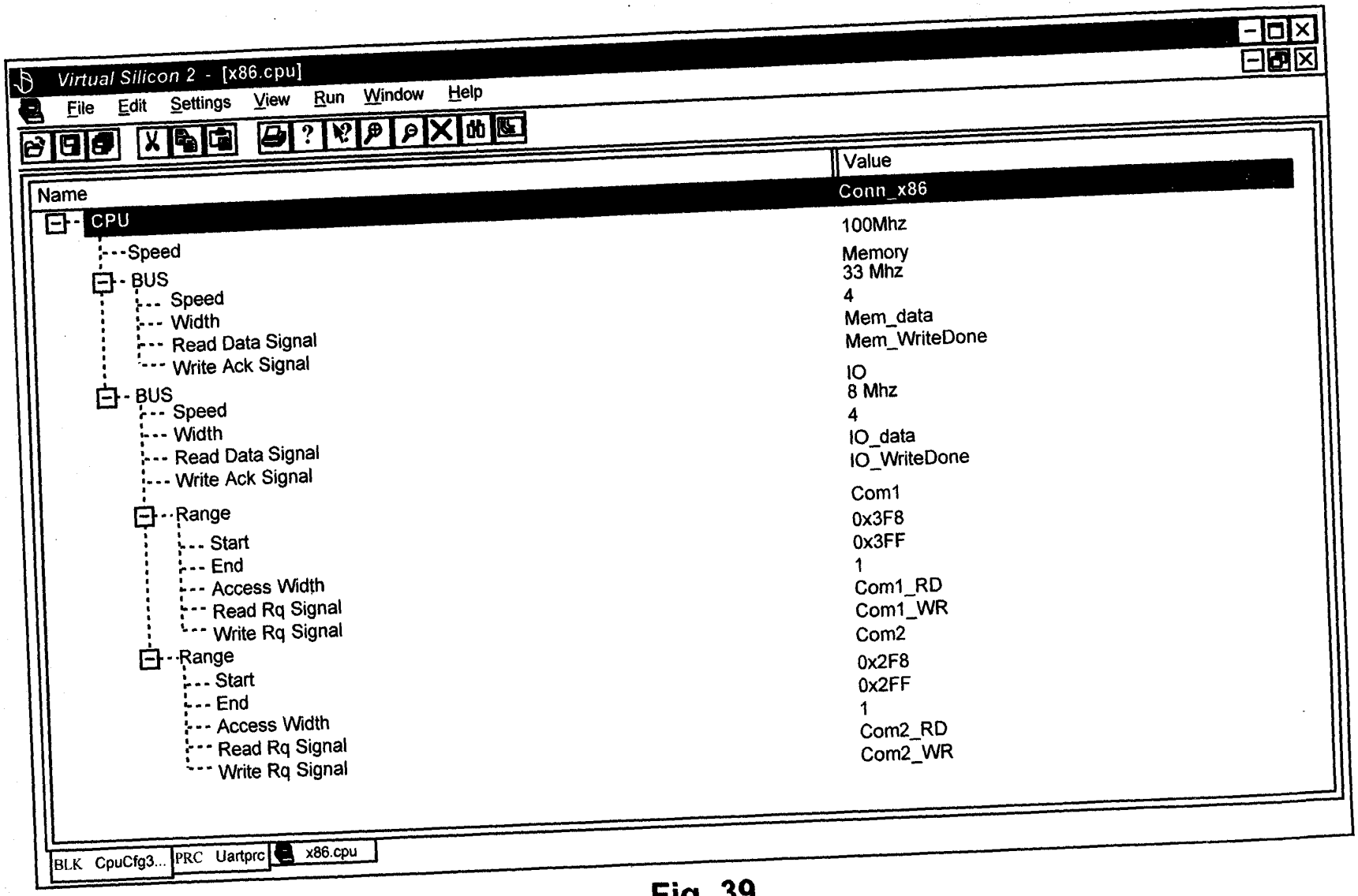
Virtual Silicon 2 - [x86.cpu]
File Edit Settings View Run Window Help
Name
Value
Conn_x86
CPU
100Mhz
Speed
Memory
BUS
33 Mhz
Speed
4
Width
Mem_data
Read Data Signal
Mem_WriteDone
Write Ack Signal
IO
BUS
8 Mhz
Speed
4
Width
IO_data
Read Data Signal
IO_WriteDone
Write Ack Signal
Com1
Range
0x3F8
Start
0x3FF
End
1
Access Width
Com1_RD
Read Rq Signal
Com1_WR
Write Rq Signal
Com2
Range
0x2F8
Start
0x2FF
End
1
Access Width
Com2_RD
Read Rq Signal
Com2_WR
Write Rq Signal
BLK CpuCfg3...
PRC Uartprc
x86.cpu

Fig. 39

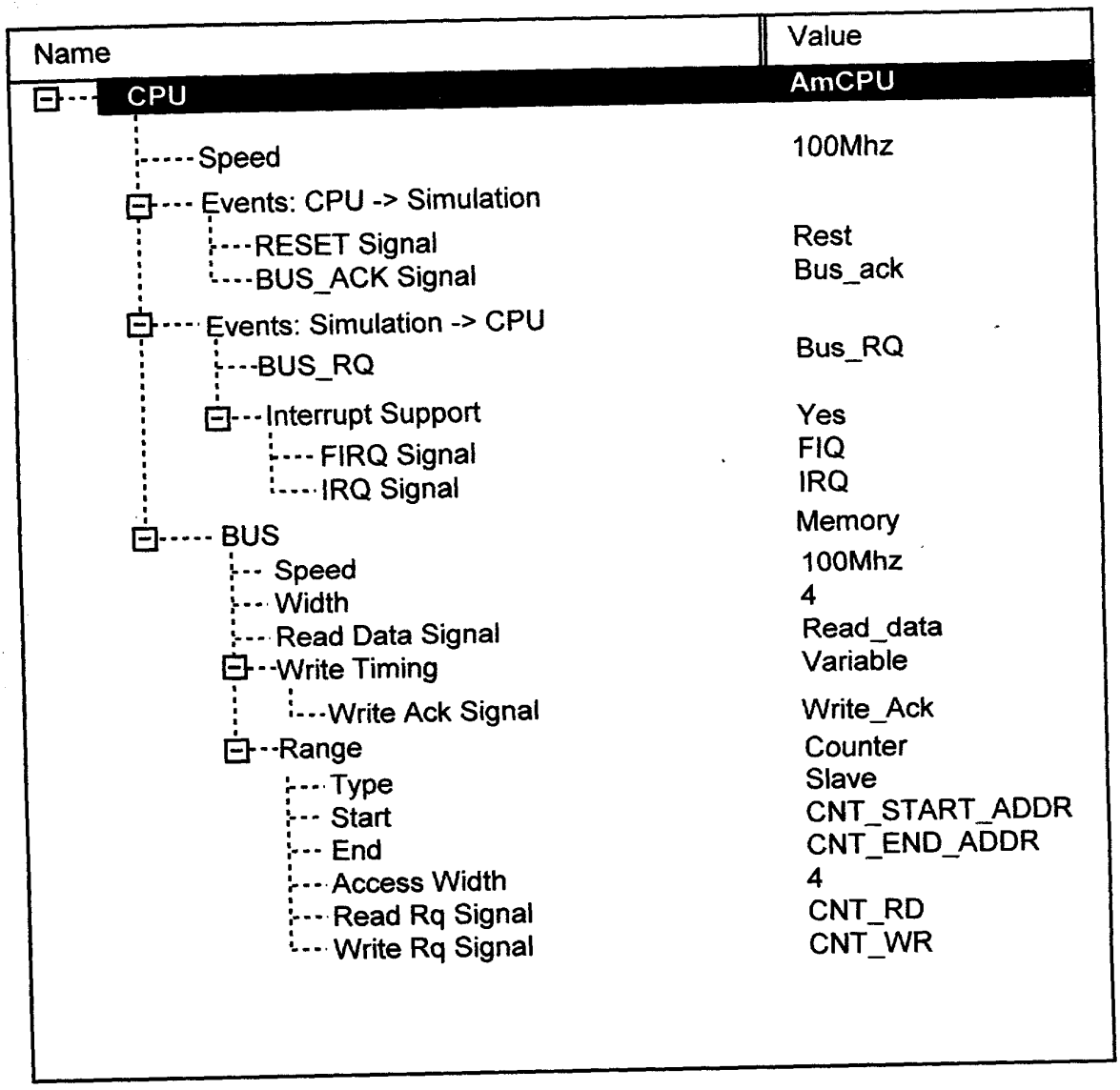
Name
Value
CPU
AmCPU
Speed
100Mhz
Events: CPU -> Simulation
RESET Signal
Rest
BUS_ACK Signal
Bus_ack
Events: Simulation -> CPU
BUS_RQ
Bus_RQ
Interrupt Support
Yes
FIRQ Signal
FIQ
IRQ Signal
IRQ
BUS
Memory
Speed
100Mhz
Width
4
Read Data Signal
Read_data
Write Timing
Variable
Write Ack Signal
Write_Ack
Range
Counter
Type
Slave
Start
CNT_START_ADDR
End
CNT_END_ADDR
Access Width
4
Read Rq Signal
CNT_RD
Write Rq Signal
CNT_WR

Fig. 40

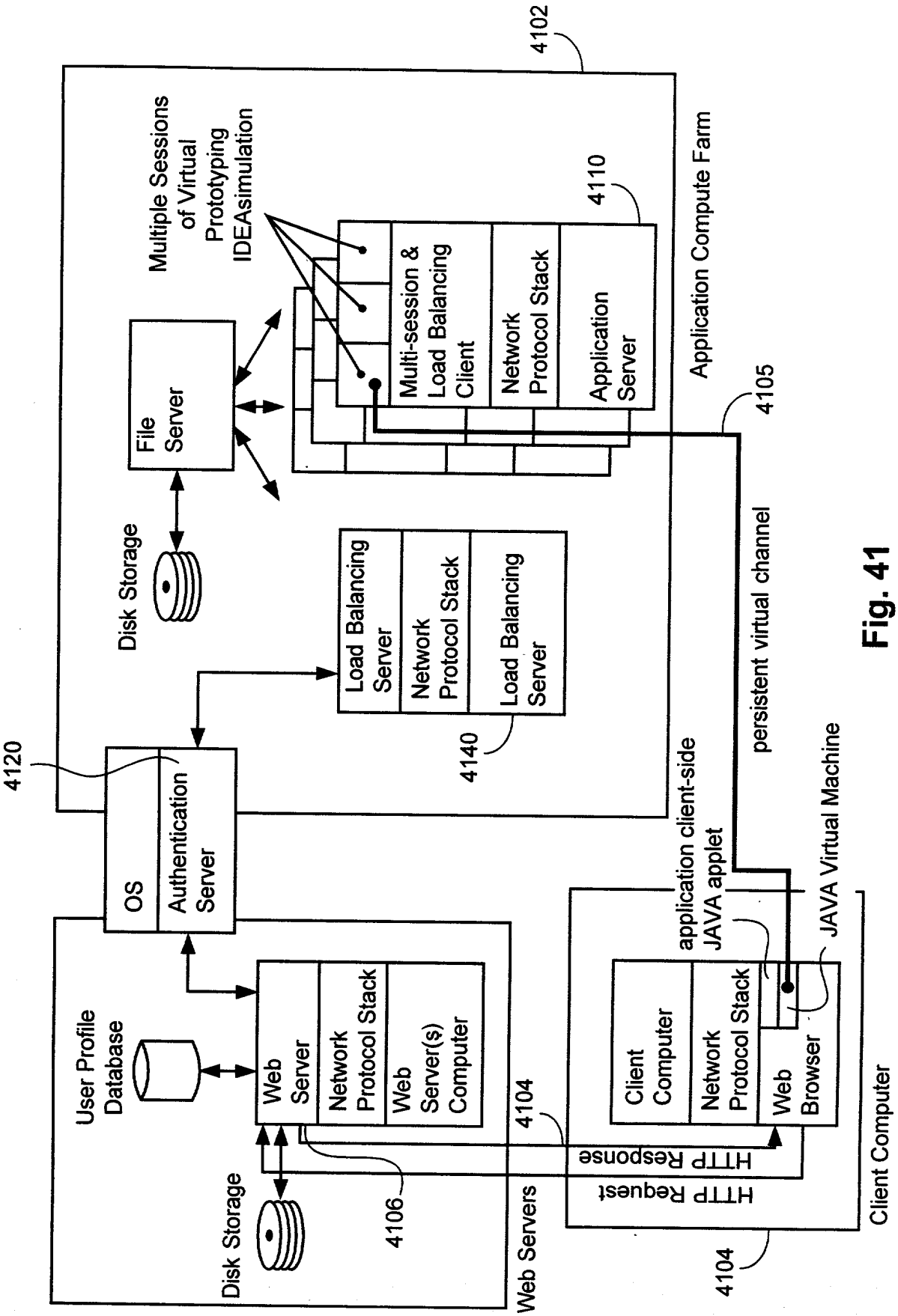
4102
Application Compute Farm
Multiple Sessions of Virtual Prototyping IDE/Asimulation
4110
Multi-session & Load Balancing Client
Network Protocol Stack
Application Server
File Server
Disk Storage
4105
persistent virtual channel
Load Balancing Server
Network Protocol Stack
Load Balancing Server
4140
4120
OS
Authentication Server
application client-side JAVA applet
JAVA Virtual Machine
User Profile Database
Web Server
Network Protocol Stack
Web Server(s) Computer
Client Computer
Network Protocol Stack
Web Browser
4104
HTTP Response
HTTP Request
4106
Disk Storage
Web Servers
Client Computer
4104

Fig. 41

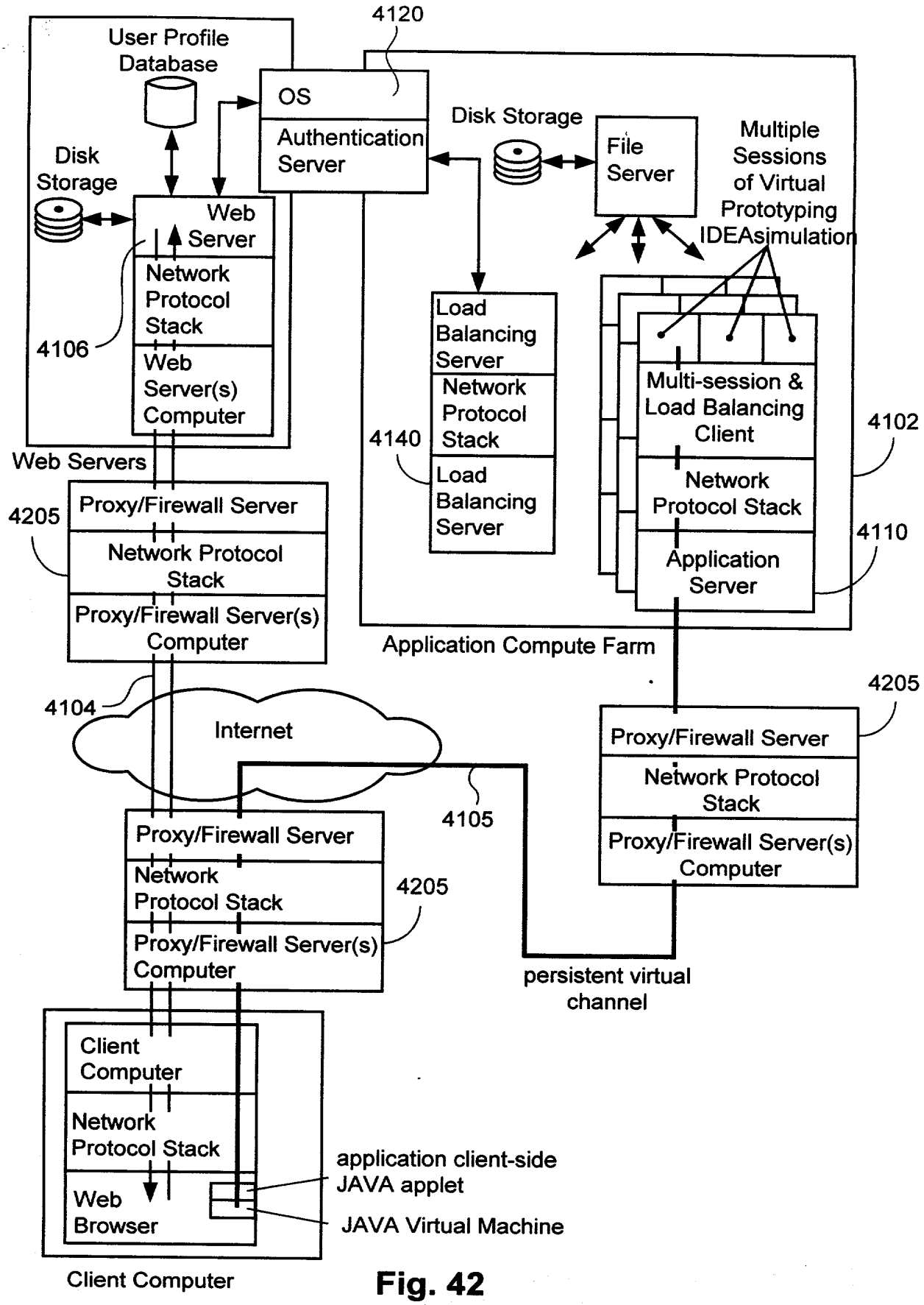
4120
User Profile Database
OS
Authentication Server
Disk Storage
File Server
Multiple Sessions of Virtual Prototyping IDEAsimulation
Disk Storage
Web Server
Network Protocol Stack
4106
Web Server(s) Computer
Load Balancing Server
Network Protocol Stack
4140
Load Balancing Server
Multi-session & Load Balancing Client
4102
Network Protocol Stack
Application Server
4110
Web Servers
4205
Proxy/Firewall Server
Network Protocol Stack
Proxy/Firewall Server(s) Computer
Application Compute Farm
4205
4104
Internet
Proxy/Firewall Server
Network Protocol Stack
Proxy/Firewall Server(s) Computer
4105
4205
persistent virtual channel
Client Computer
Network Protocol Stack
Web Browser
application client-side JAVA applet
JAVA Virtual Machine
Client Computer

Fig. 42

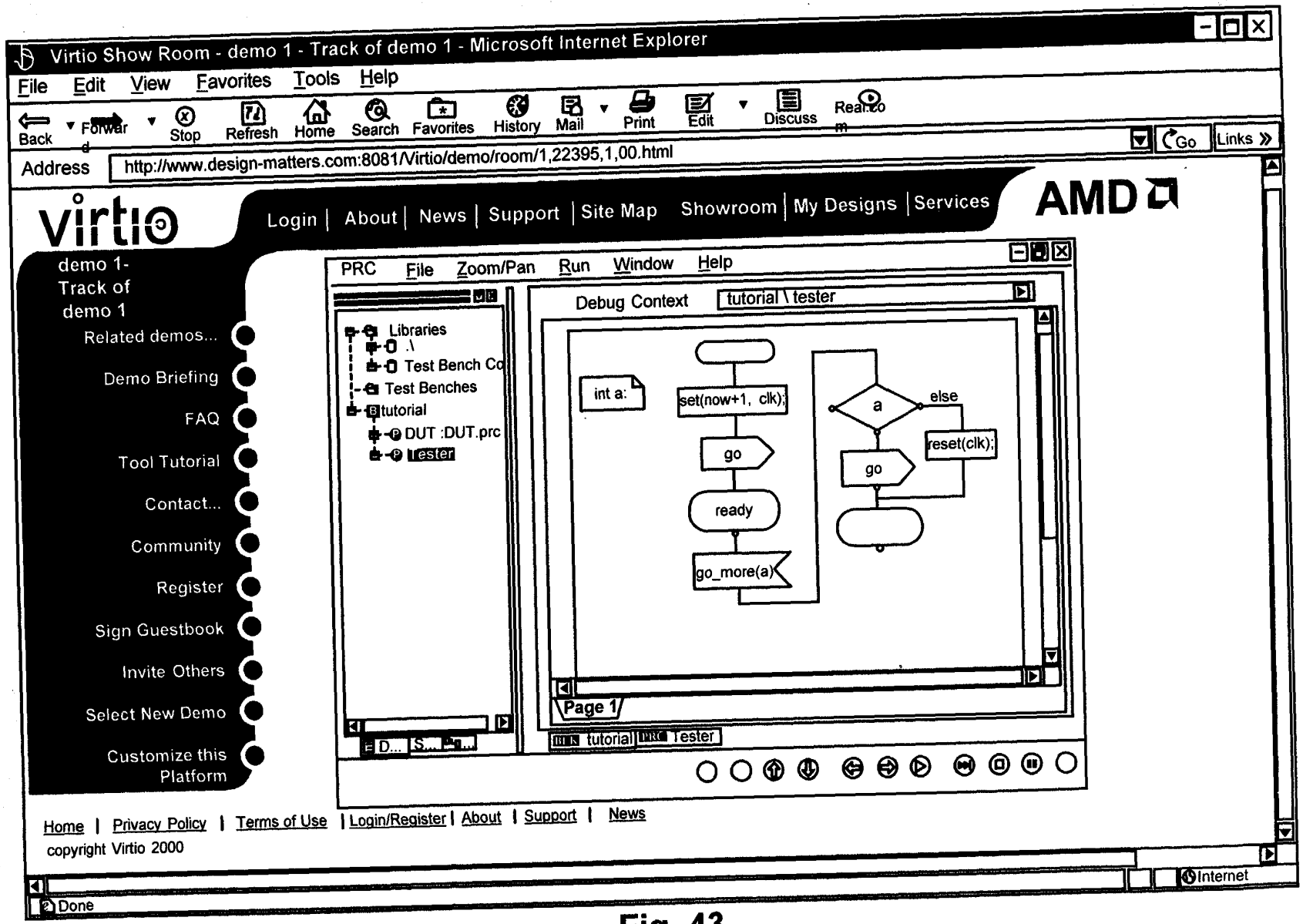

Fig. 43

Application No. 09/872,435
Title: METHOD AND SYSTEM FOR VIRTUAL PROTOTYPING
Inventor(s): Stephen L. Bade et al.
Atty. Docket No.: 22178-05012
Sheet 44 of 65

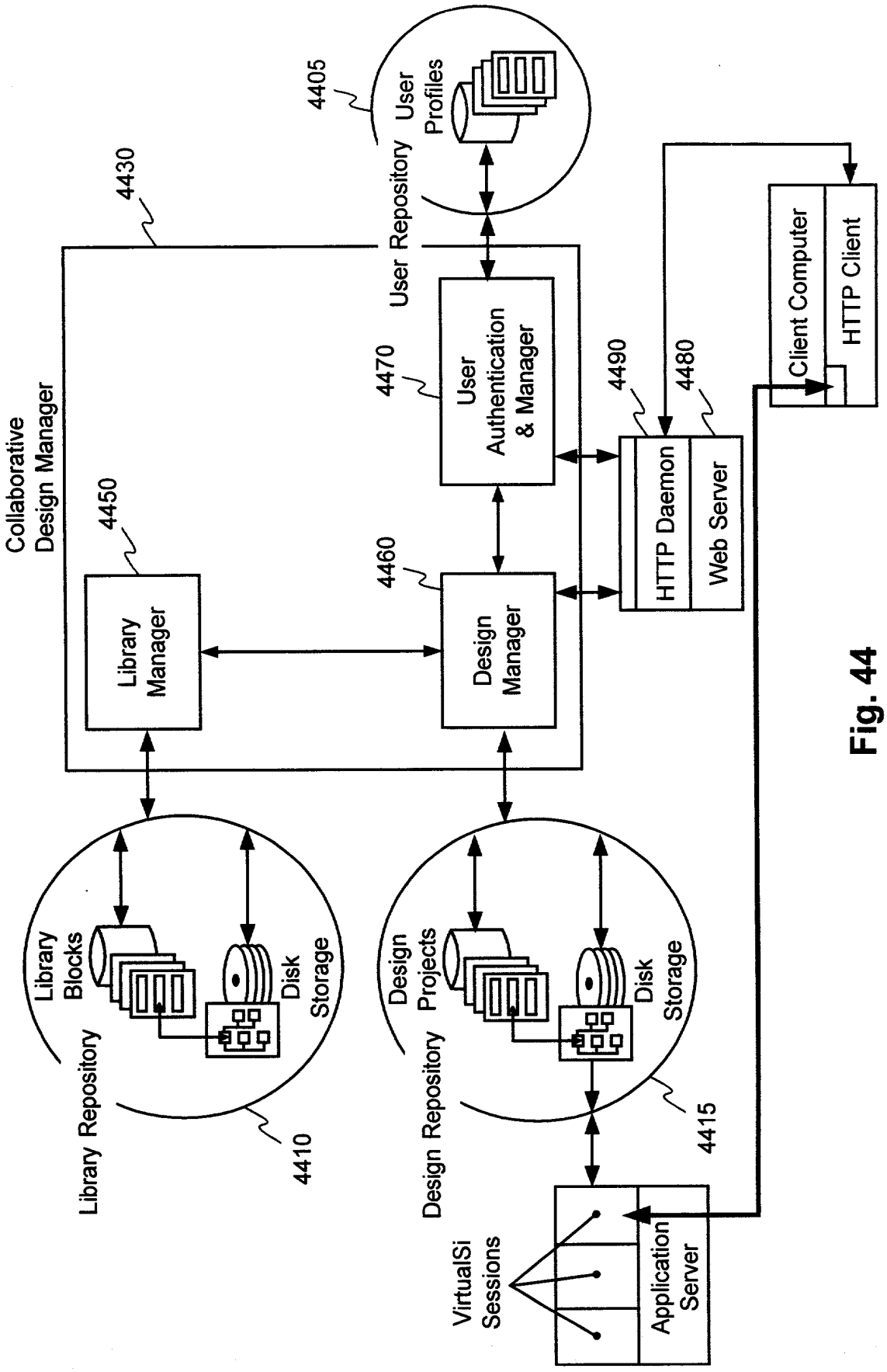
4405
User Profiles
User Repository
4430
Collaborative Design Manager
4470
User Authentication & Manager
4490
4480
Client Computer
HTTP Client
4450
Library Manager
4460
Design Manager
HTTP Daemon
Web Server
Library Blocks
Disk Storage
Library Repository
4410
Design Projects
Disk Storage
Design Repository
4415
VirtualSi Sessions
Application Server

Fig. 44

{ } Clock_1	Scope Name
clk(int)	Signal name and declaration

t	Timer or clock name and declaration
S clk	Local name of a signal coming from the upper scope (inherited)
myClk	Timer or clock is being set
	Signal is being sent
	Signal is being received
	Signal is being saved

Fig. 45

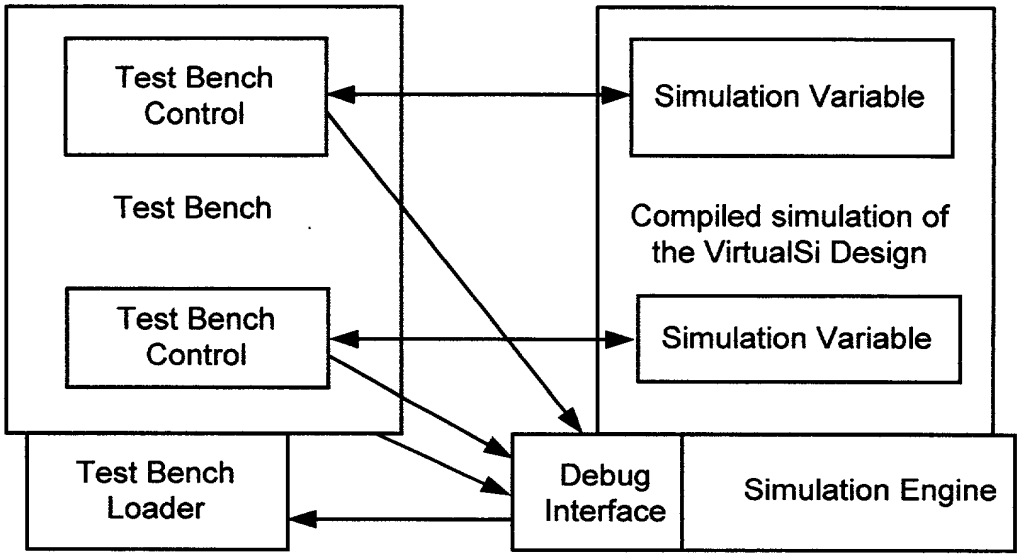
Test Bench Control
Test Bench
Test Bench Control
Test Bench Loader
Simulation Variable
Compiled simulation of the VirtualSi Design
Simulation Variable
Debug Interface
Simulation Engine

Fig. 46

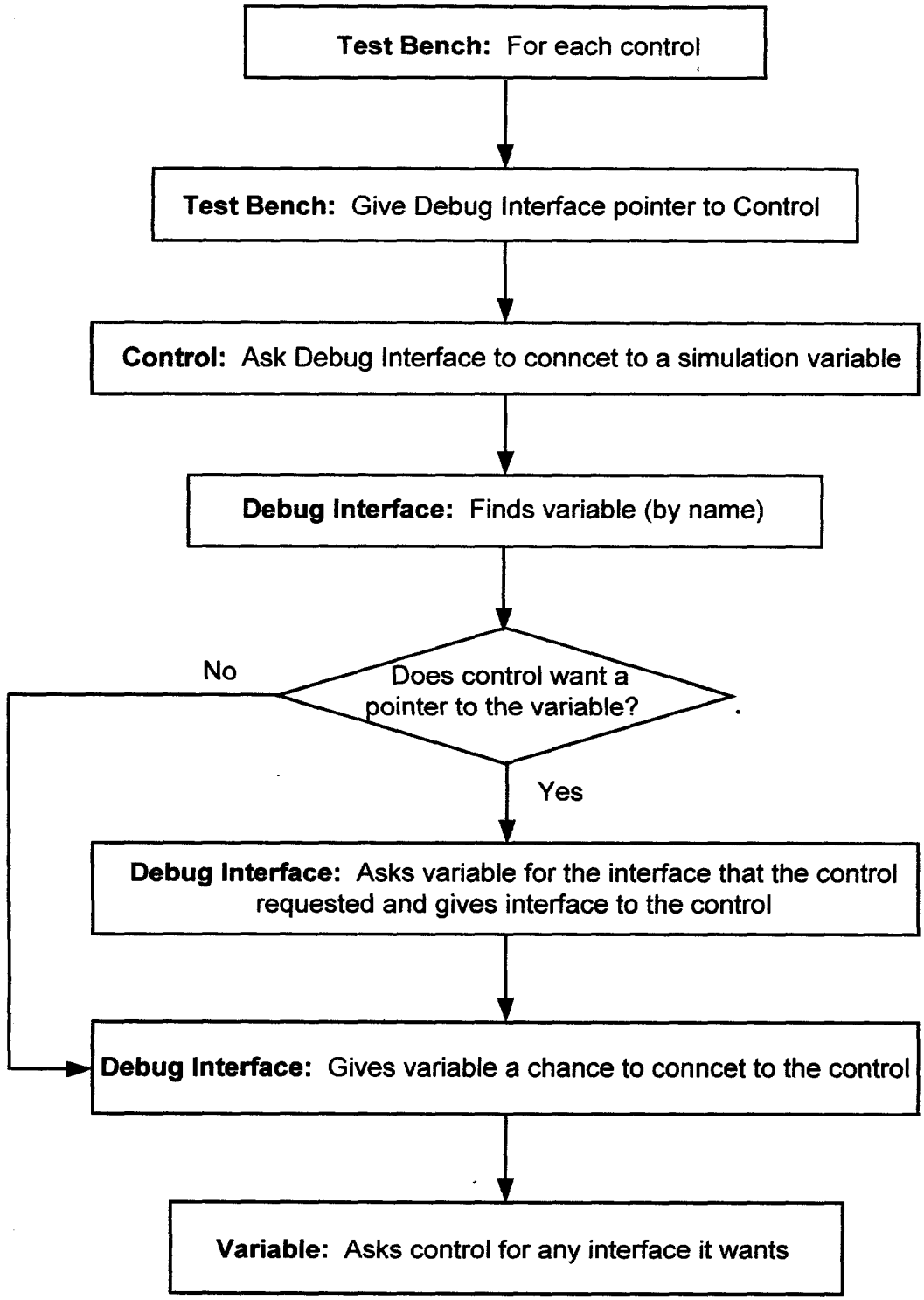
Test Bench: For each control
Test Bench: Give Debug Interface pointer to Control
Control: Ask Debug Interface to conncet to a simulation variable
Debug Interface: Finds variable (by name)
Does control want a pointer to the variable?
No
Yes
Debug Interface: Asks variable for the interface that the control requested and gives interface to the control
Debug Interface: Gives variable a chance to conncet to the control
Variable: Asks control for any interface it wants

Fig. 47

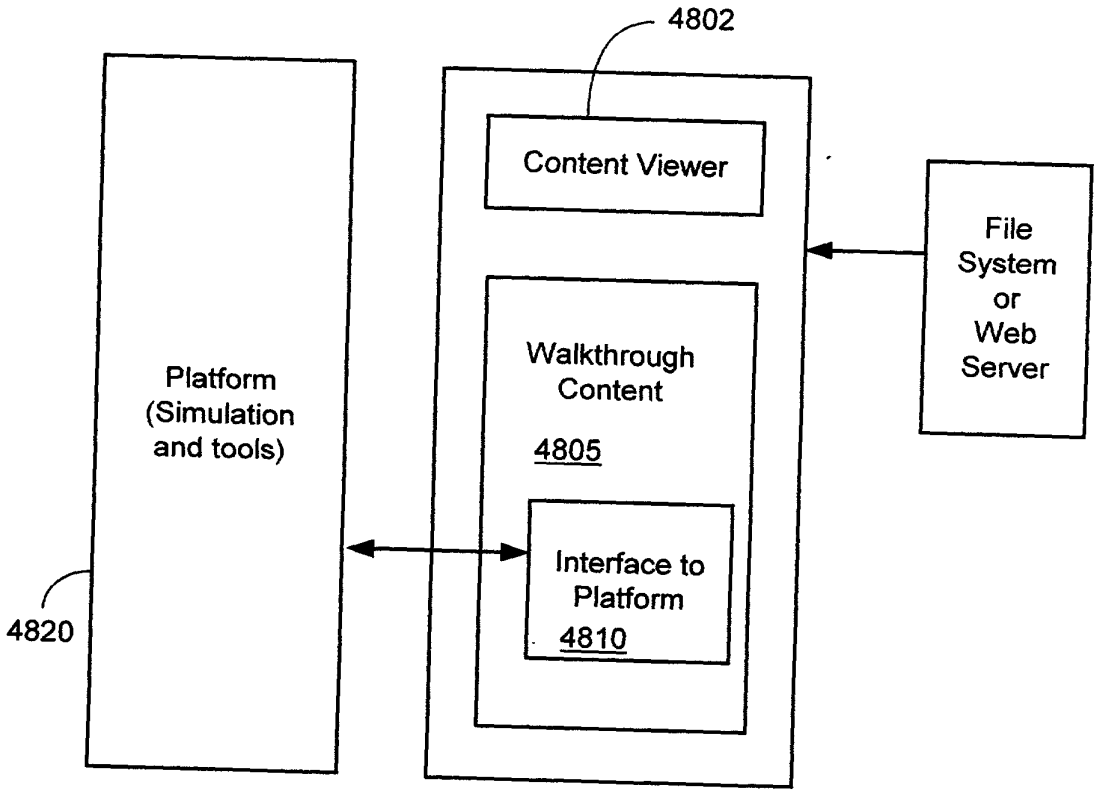
4802
Content Viewer
File System or Web Server
Walkthrough Content
4805
Platform (Simulation and tools)
Interface to Platform
4810
4820

Fig. 48

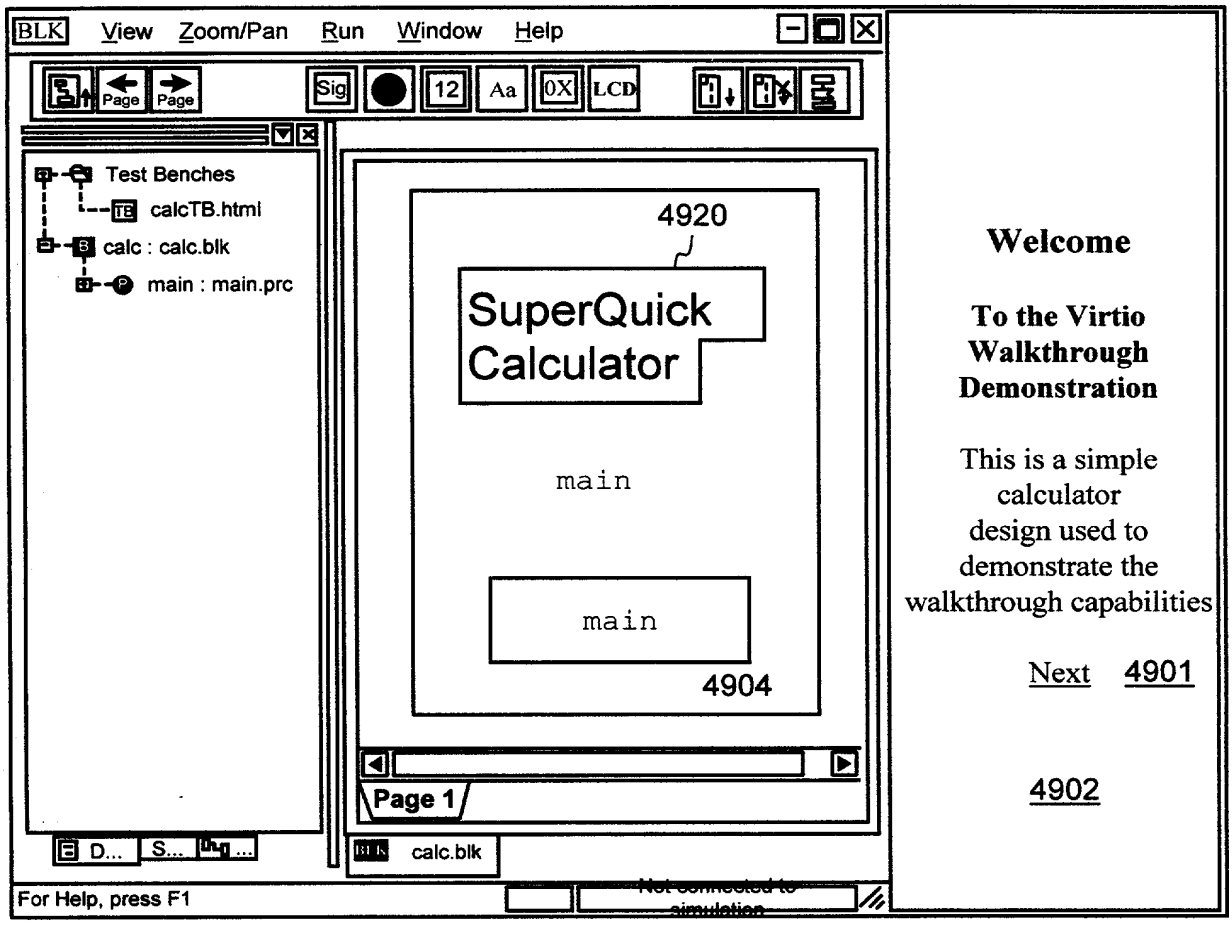
BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Test Benches
calcTB.html
calc : calc.blk
main : main.prc
4920
SuperQuick Calculator
main
main
4904
Page 1
calc.blk
D...
S...
For Help, press F1
Welcome
To the Virtio Walkthrough Demonstration
This is a simple calculator design used to demonstrate the walkthrough capabilities
Next 4901
4902

Fig. 49A

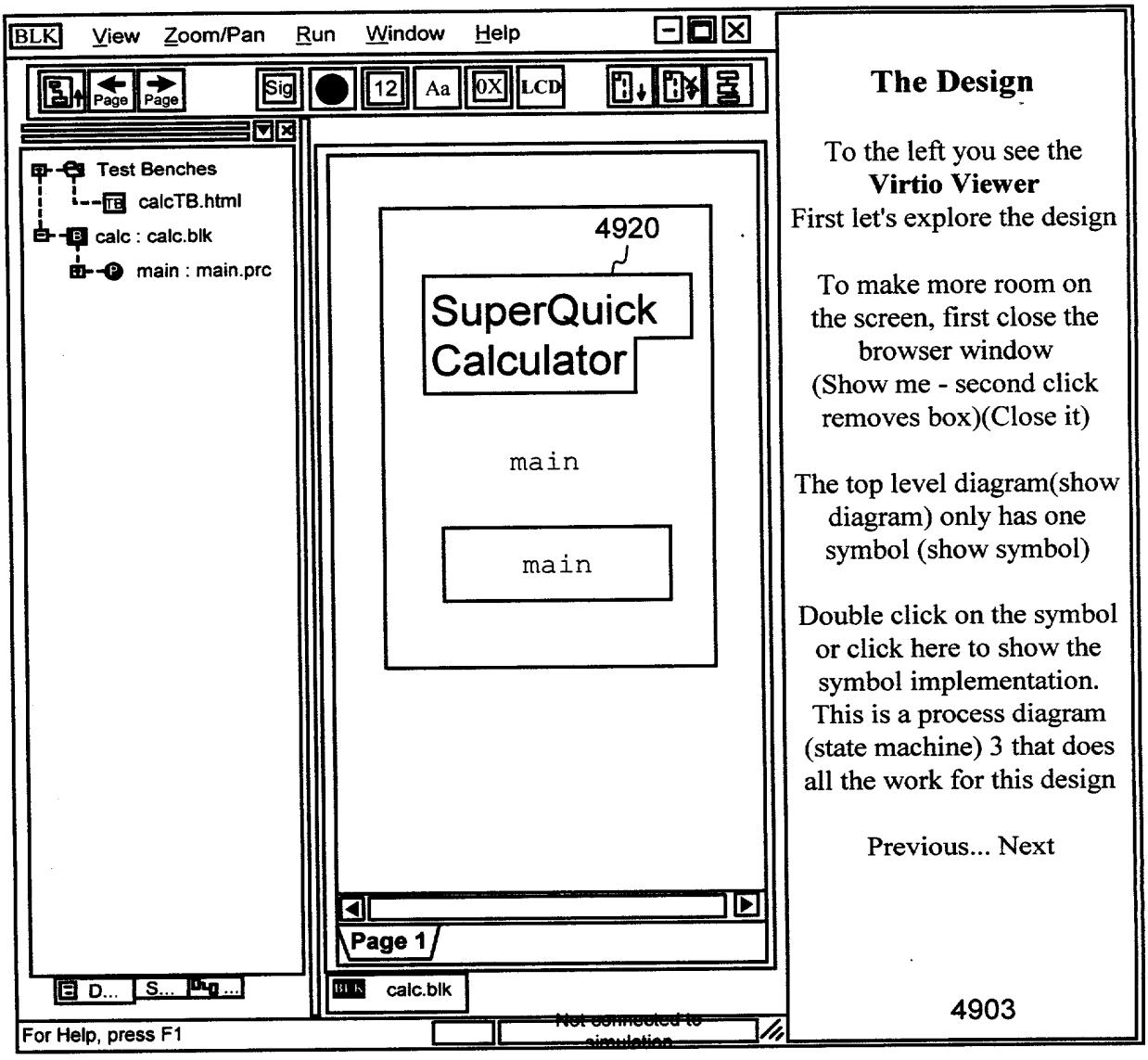
BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Test Benches
calcTB.html
calc : calc.blk
main : main.prc
4920
SuperQuick Calculator
main
main
Page 1
calc.blk
D...
S...
For Help, press F1
The Design
To the left you see the Virtio Viewer
First let's explore the design
To make more room on the screen, first close the browser window
(Show me - second click removes box)(Close it)
The top level diagram(show diagram) only has one symbol (show symbol)
Double click on the symbol or click here to show the symbol implementation.
This is a process diagram (state machine) 3 that does all the work for this design
Previous... Next
4903

Fig. 49B

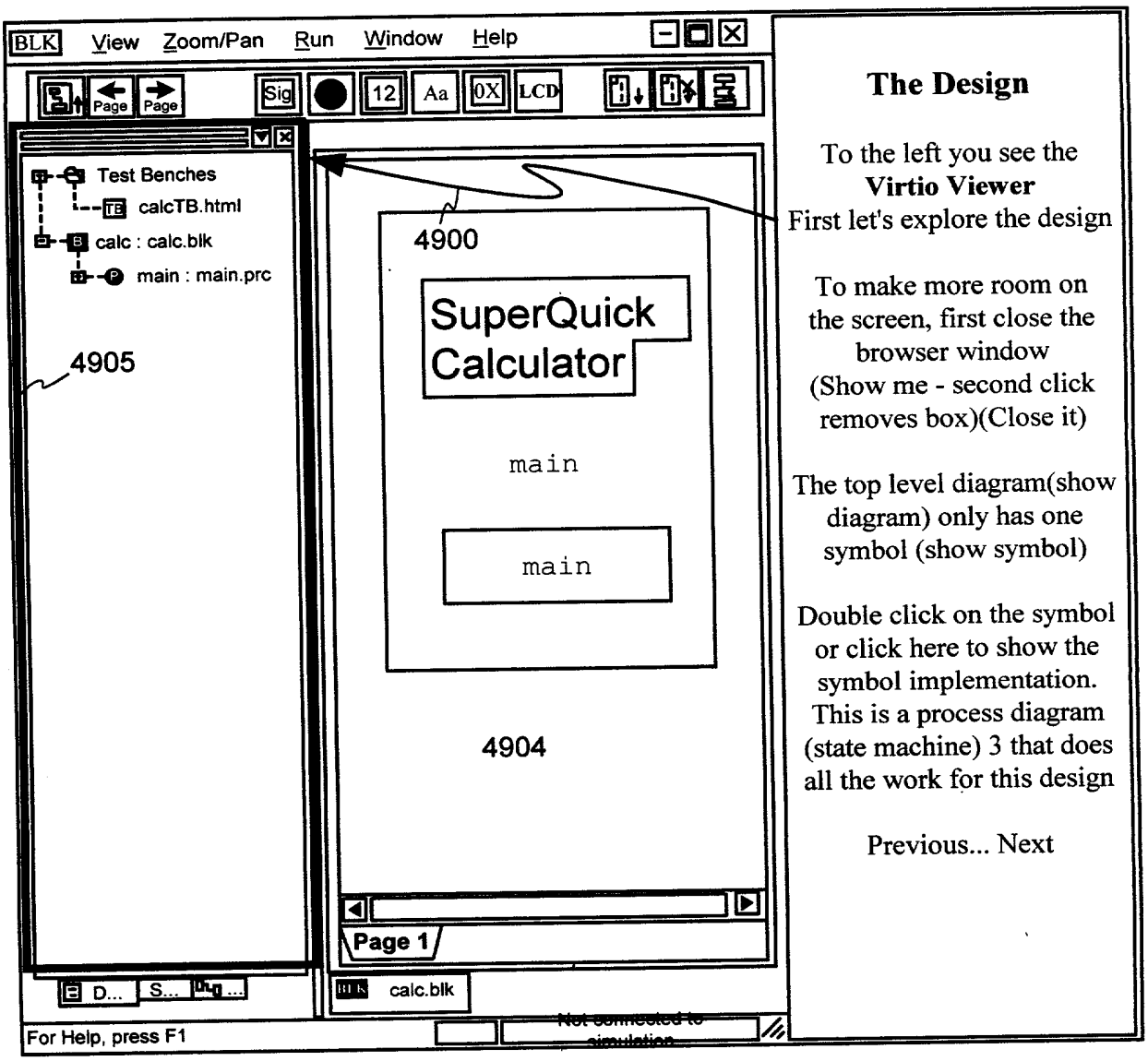
BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Test Benches
calcTB.html
calc : calc.blk
main : main.prc
4905
4900
SuperQuick Calculator
main
main
4904
Page 1
calc.blk
D...
S...
For Help, press F1
The Design
To the left you see the Virtio Viewer First let's explore the design
To make more room on the screen, first close the browser window (Show me - second click removes box)(Close it)
The top level diagram(show diagram) only has one symbol (show symbol)
Double click on the symbol or click here to show the symbol implementation. This is a process diagram (state machine) 3 that does all the work for this design
Previous... Next

Fig. 49C

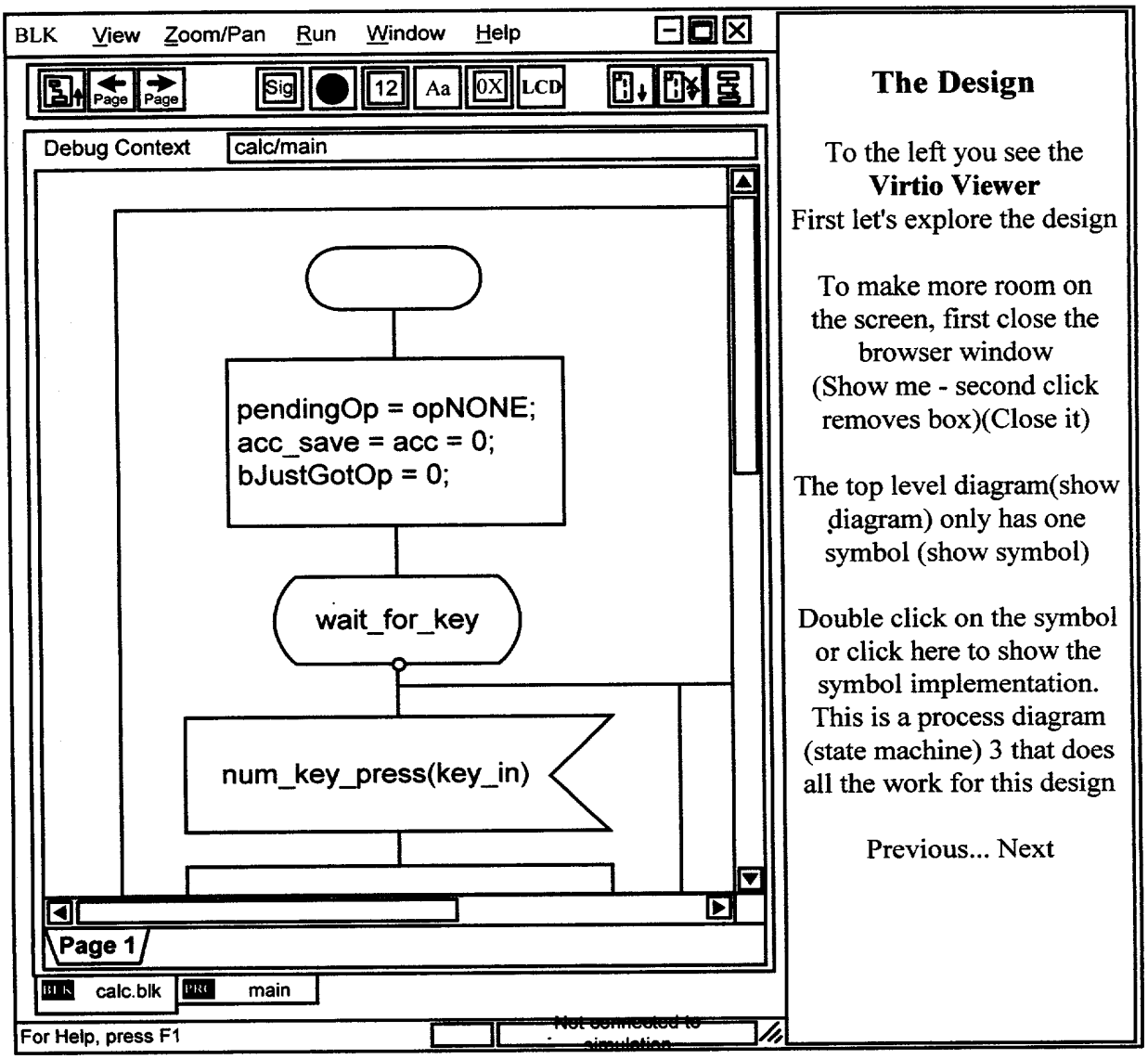
BLK View Zoom/Pan Run Window Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
pendingOp = opNONE;
acc_save = acc = 0;
bJustGotOp = 0;
wait_for_key
num_key_press(key_in)
Page 1
BLK calc.blk
PRG main
For Help, press F1
The Design
To the left you see the Virtio Viewer First let's explore the design
To make more room on the screen, first close the browser window (Show me - second click removes box)(Close it)
The top level diagram(show diagram) only has one symbol (show symbol)
Double click on the symbol or click here to show the symbol implementation. This is a process diagram (state machine) 3 that does all the work for this design
Previous... Next

Fig. 49D

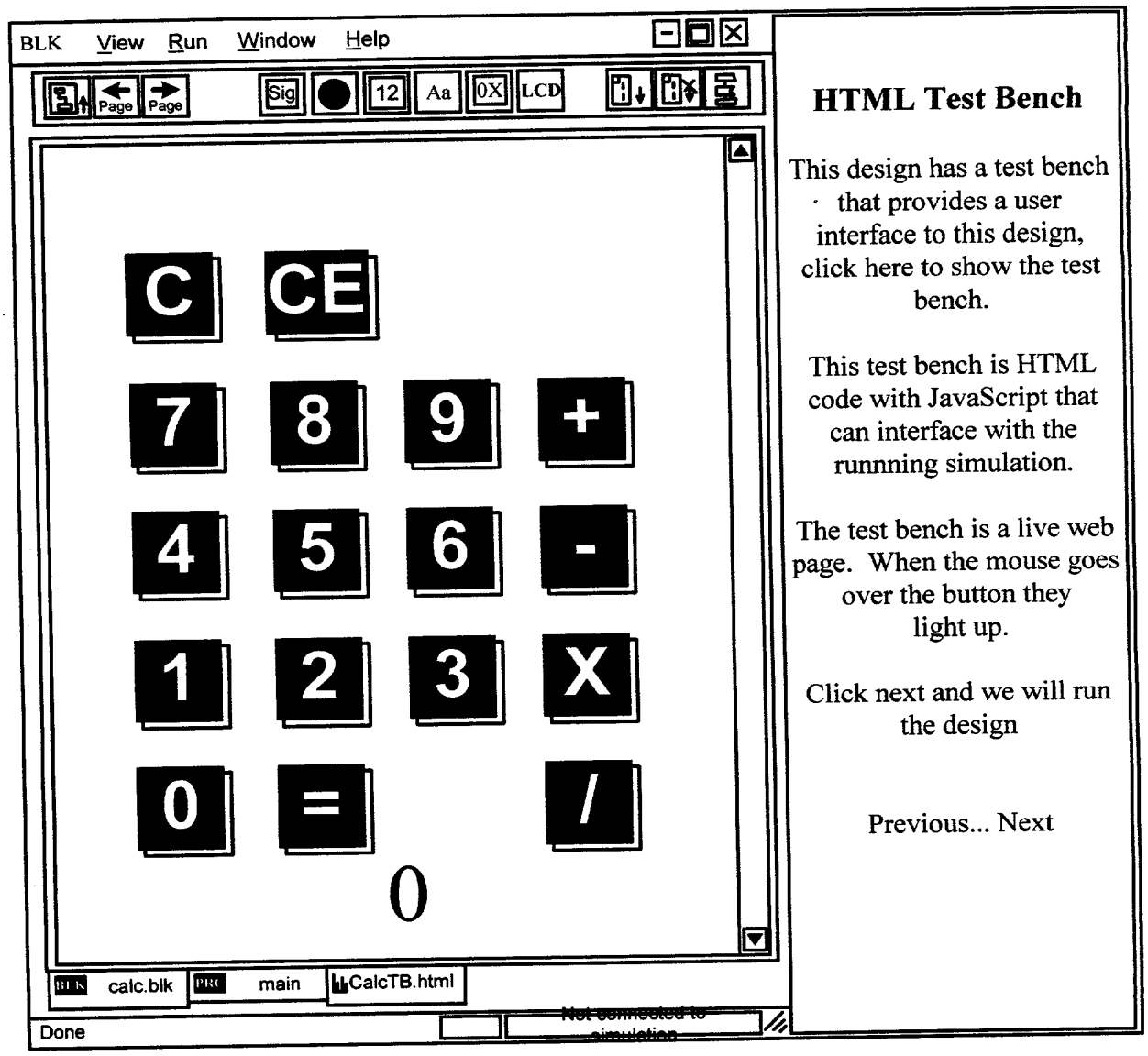
BLK View Run Window Help
Page
Page
Sig
12
Aa
0X
LCD
C
CE
7
8
9
+
4
5
6
-
1
2
3
X
0
=
/
0
calc.blk
main
CalcTB.html
Done
HTML Test Bench
This design has a test bench that provides a user interface to this design, click here to show the test bench.
This test bench is HTML code with JavaScript that can interface with the runnning simulation.
The test bench is a live web page. When the mouse goes over the button they light up.
Click next and we will run the design
Previous... Next

Fig. 49E

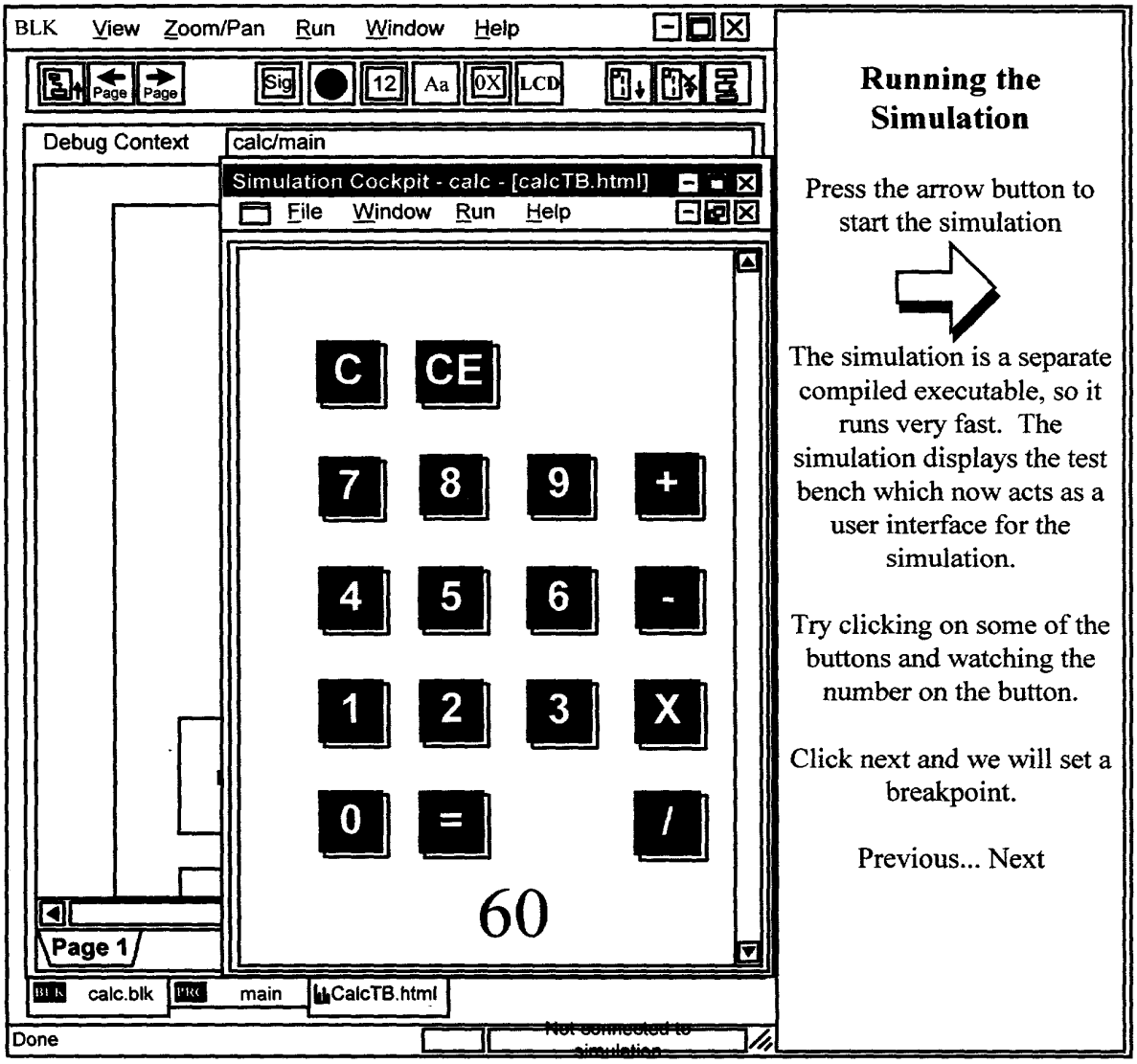
BLK View Zoom/Pan Run Window Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
Simulation Cockpit - calc - [calcTB.html]
File Window Run Help
C
CE
7
8
9
+
4
5
6
-
1
2
3
X
0
=
/
60
Page 1
calc.blk
main
CalcTB.html
Done
Not connected to simulation
Running the Simulation
Press the arrow button to start the simulation
The simulation is a separate compiled executable, so it runs very fast. The simulation displays the test bench which now acts as a user interface for the simulation.
Try clicking on some of the buttons and watching the number on the button.
Click next and we will set a breakpoint.
Previous... Next

Fig. 49F

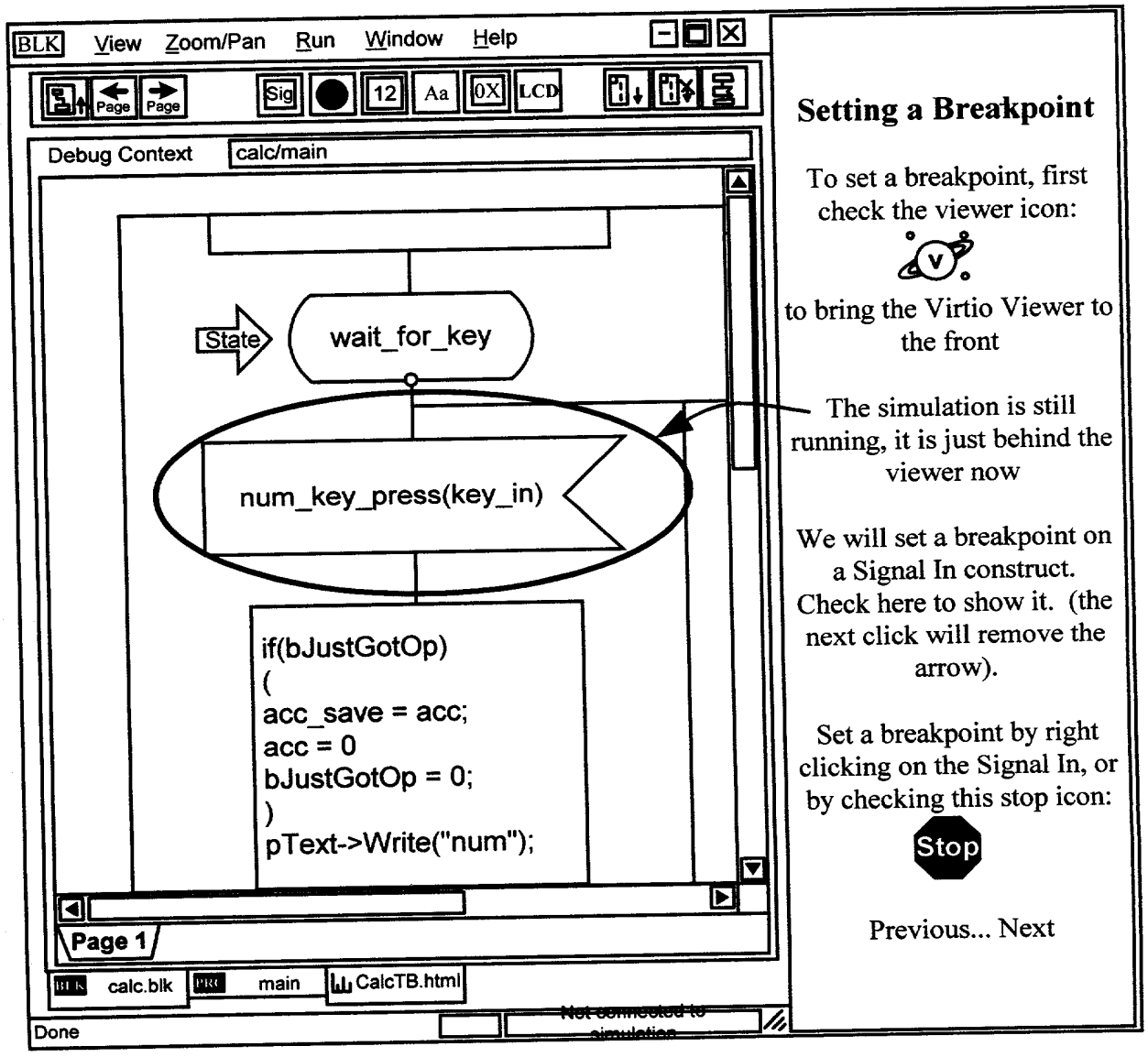
BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
State
wait_for_key
num_key_press(key_in)
if(bJustGotOp)
(
acc_save = acc;
acc = 0
bJustGotOp = 0;
)
pText->Write("num");
Page 1
calc.blk
main
CalcTB.html
Done
Setting a Breakpoint
To set a breakpoint, first check the viewer icon:
to bring the Virtio Viewer to the front
The simulation is still running, it is just behind the viewer now
We will set a breakpoint on a Signal In construct. Check here to show it. (the next click will remove the arrow).
Set a breakpoint by right clicking on the Signal In, or by checking this stop icon:
Stop
Previous... Next

Fig. 49G

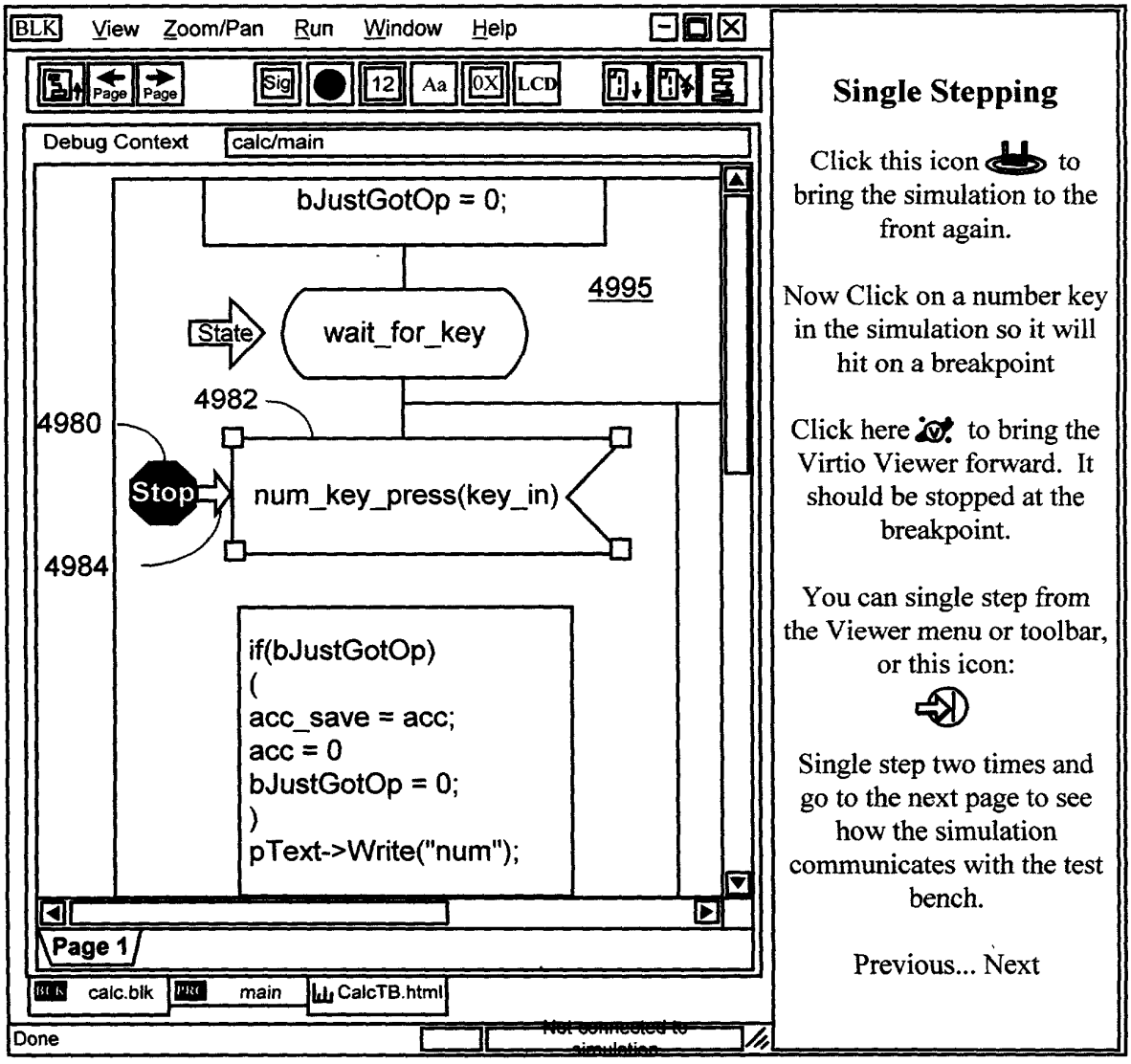
BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
bJustGotOp = 0;
4995
State
wait_for_key
4982
4980
Stop
num_key_press(key_in)
4984
if(bJustGotOp)
(
acc_save = acc;
acc = 0
bJustGotOp = 0;
)
pText->Write("num");
Page 1
calc.blk
main
CalcTB.html
Done
Single Stepping
Click this icon to bring the simulation to the front again.
Now Click on a number key in the simulation so it will hit on a breakpoint
Click here to bring the Virtio Viewer forward. It should be stopped at the breakpoint.
You can single step from the Viewer menu or toolbar, or this icon:
Single step two times and go to the next page to see how the simulation communicates with the test bench.
Previous... Next

Fig. 49H

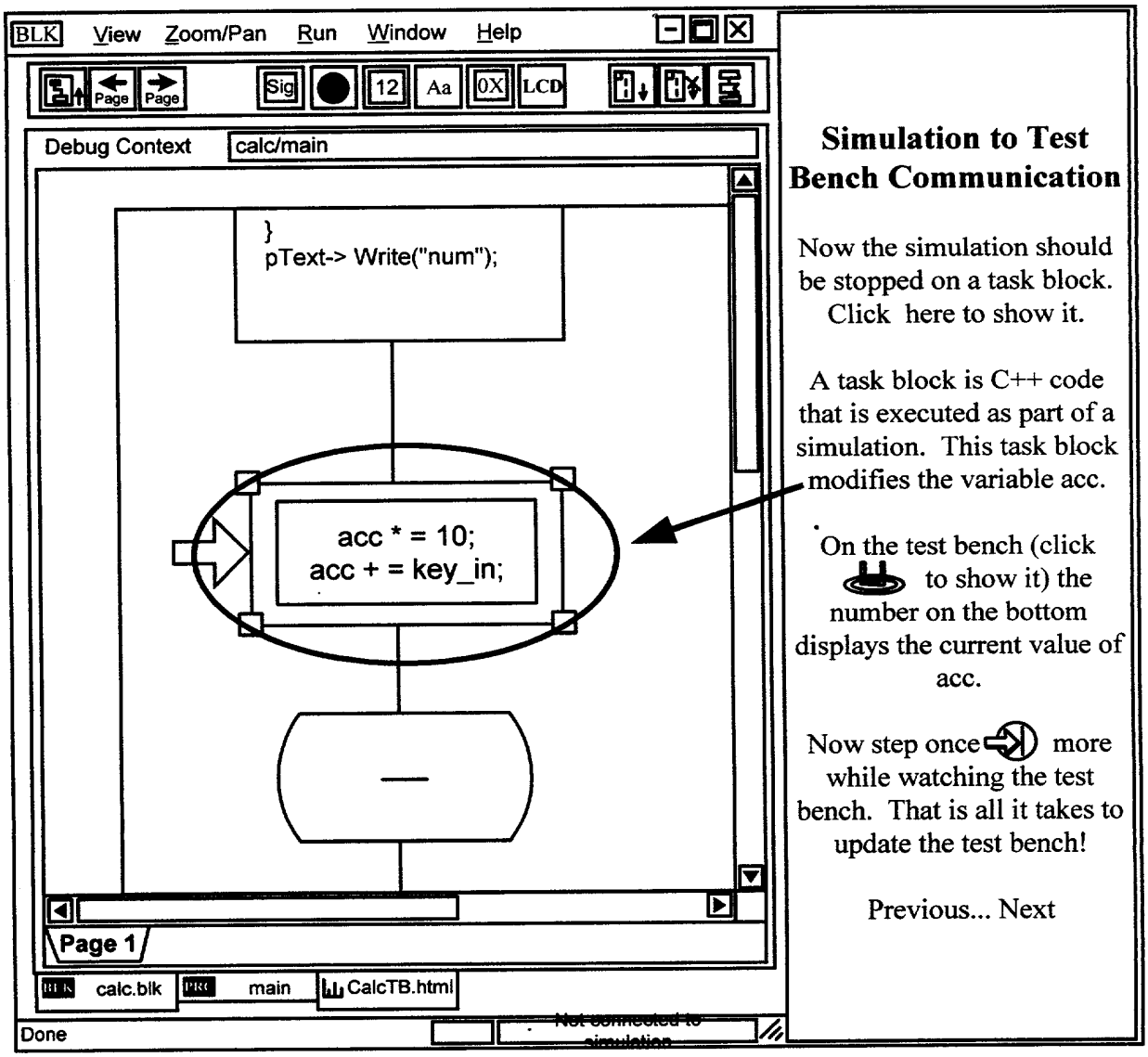
BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
calc/main
}
pText-> Write("num");
acc * = 10;
acc + = key_in;
Page 1
calc.blk
main
CalcTB.html
Done
Not connected to simulation
Simulation to Test Bench Communication
Now the simulation should be stopped on a task block. Click here to show it.
A task block is C++ code that is executed as part of a simulation. This task block modifies the variable acc.
On the test bench (click to show it) the number on the bottom displays the current value of acc.
Now step once more while watching the test bench. That is all it takes to update the test bench!
Previous... Next

Fig. 49l

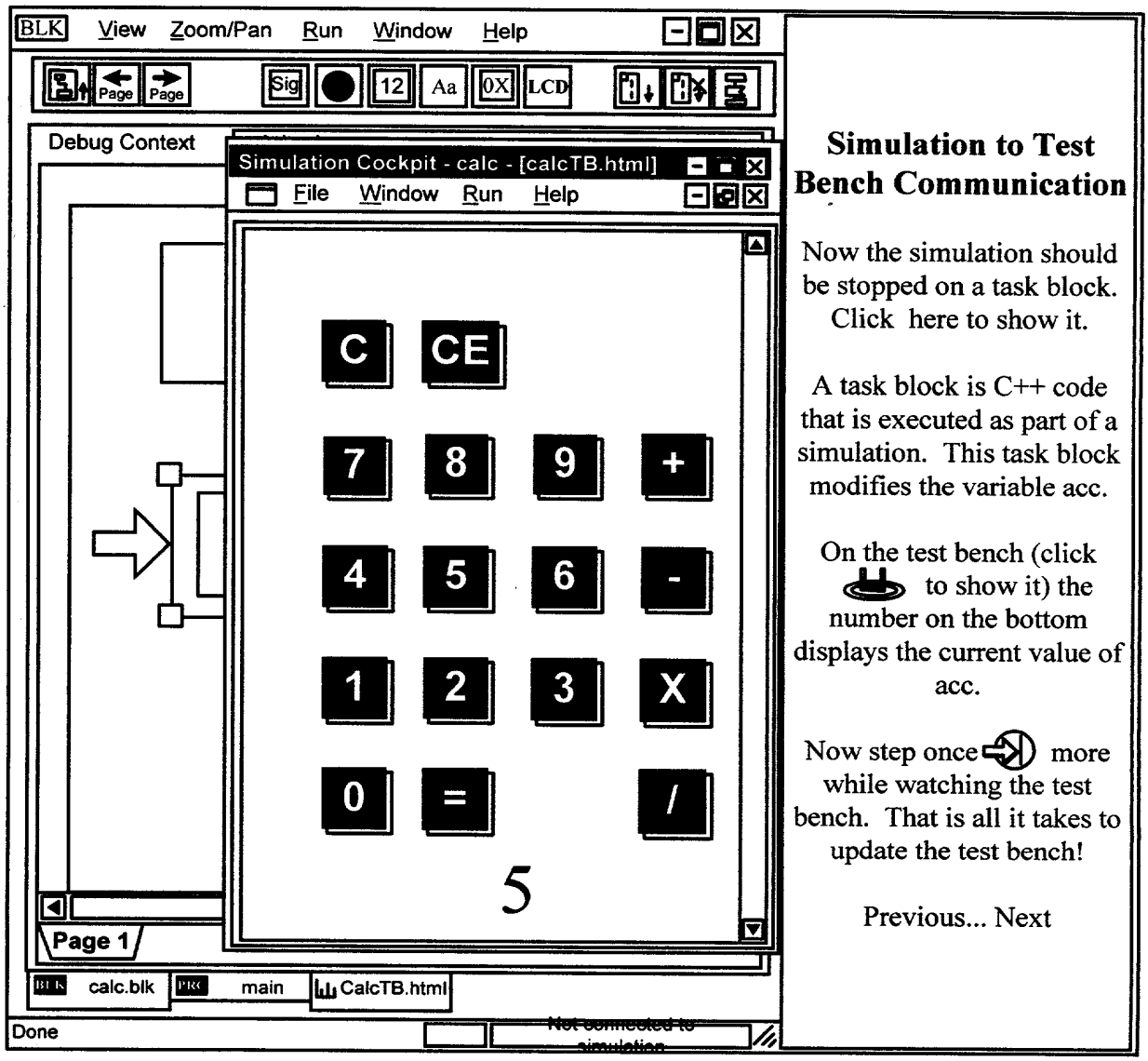
BLK
View
Zoom/Pan
Run
Window
Help
Page
Page
Sig
12
Aa
0X
LCD
Debug Context
Simulation Cockpit - calc - [calcTB.html]
File
Window
Run
Help
C
CE
7
8
9
+
4
5
6
-
1
2
3
X
0
=
/
5
Page 1
calc.blk
main
CalcTB.html
Done
Simulation to Test Bench Communication
Now the simulation should be stopped on a task block. Click here to show it.
A task block is C++ code that is executed as part of a simulation. This task block modifies the variable acc.
On the test bench (click to show it) the number on the bottom displays the current value of acc.
Now step once more while watching the test bench. That is all it takes to update the test bench!
Previous... Next

Fig. 49J

Integrator Lab Screen Snap Shots - On-Line Enablement

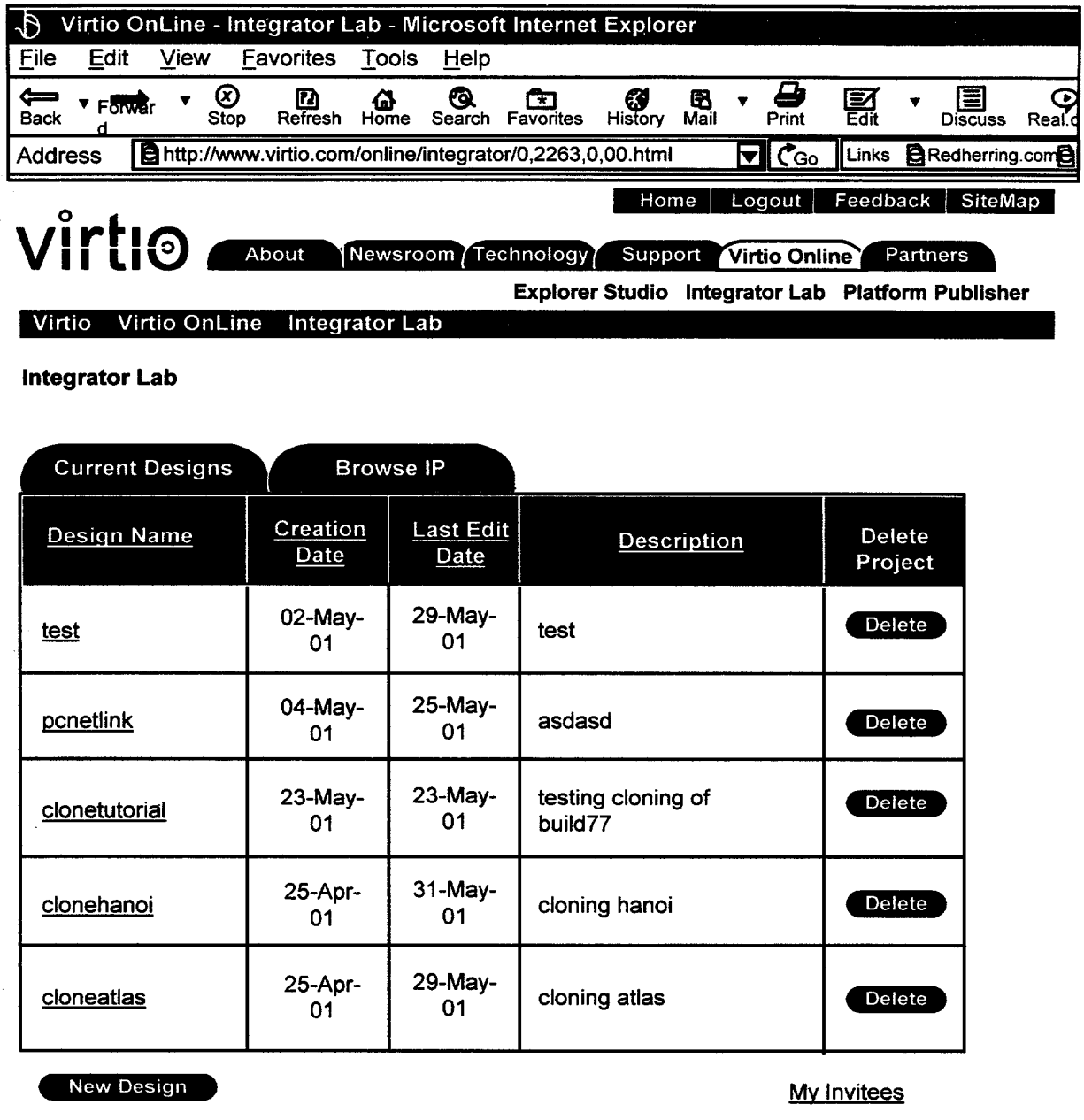

Fig. 50

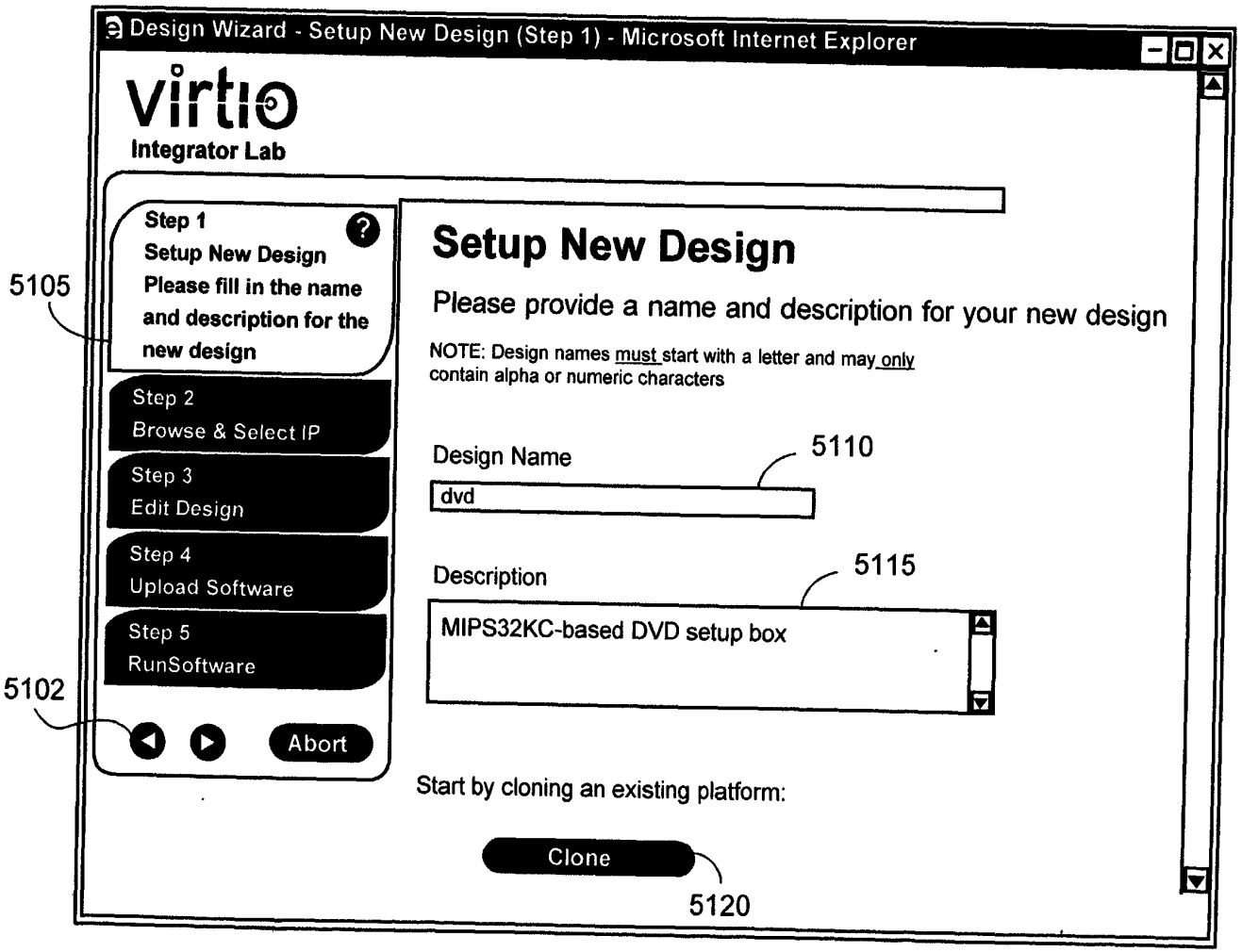

Fig. 51

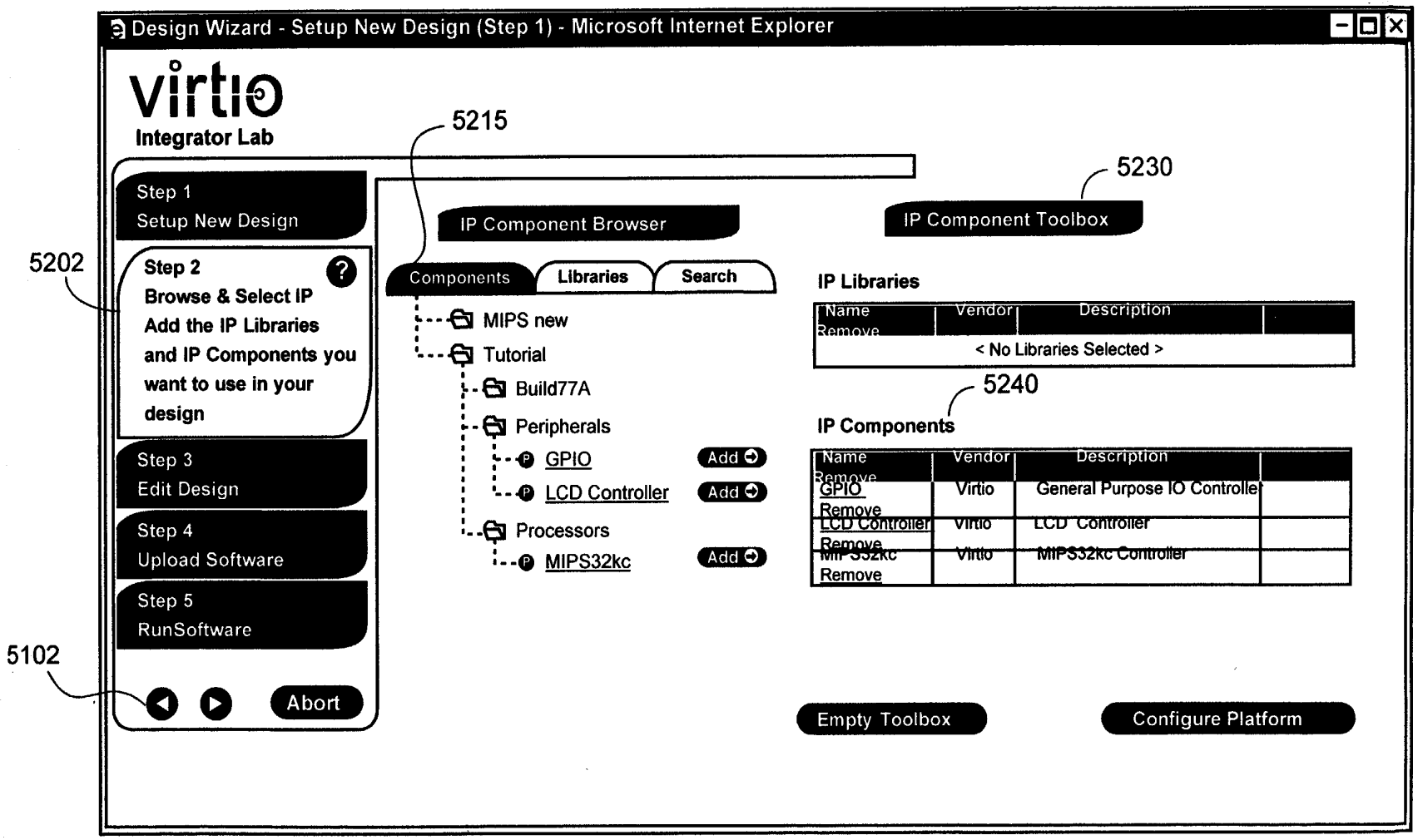
Design Wizard - Setup New Design (Step 1) - Microsoft Internet Explorer
virtio
Integrator Lab
5215
5230
Step 1
Setup New Design
IP Component Browser
IP Component Toolbox
5202
Step 2
Browse & Select IP
Add the IP Libraries
and IP Components you
want to use in your
design
Components
Libraries
Search
IP Libraries
Name
Vendor
Description
Remove
< No Libraries Selected >
MIPS new
Tutorial
Build77A
Peripherals
GPIO
Add
LCD Controller
Add
Processors
MIPS32kc
Add
5240
IP Components
Name
Vendor
Description
GPIO
Remove
Virtio
General Purpose IO Controller
LCD Controller
Remove
Virtio
LCD Controller
MIPS32kc
Remove
Virtio
MIPS32kc Controller
Step 3
Edit Design
Step 4
Upload Software
Step 5
RunSoftware
5102
Abort
Empty Toolbox
Configure Platform

Fig. 52

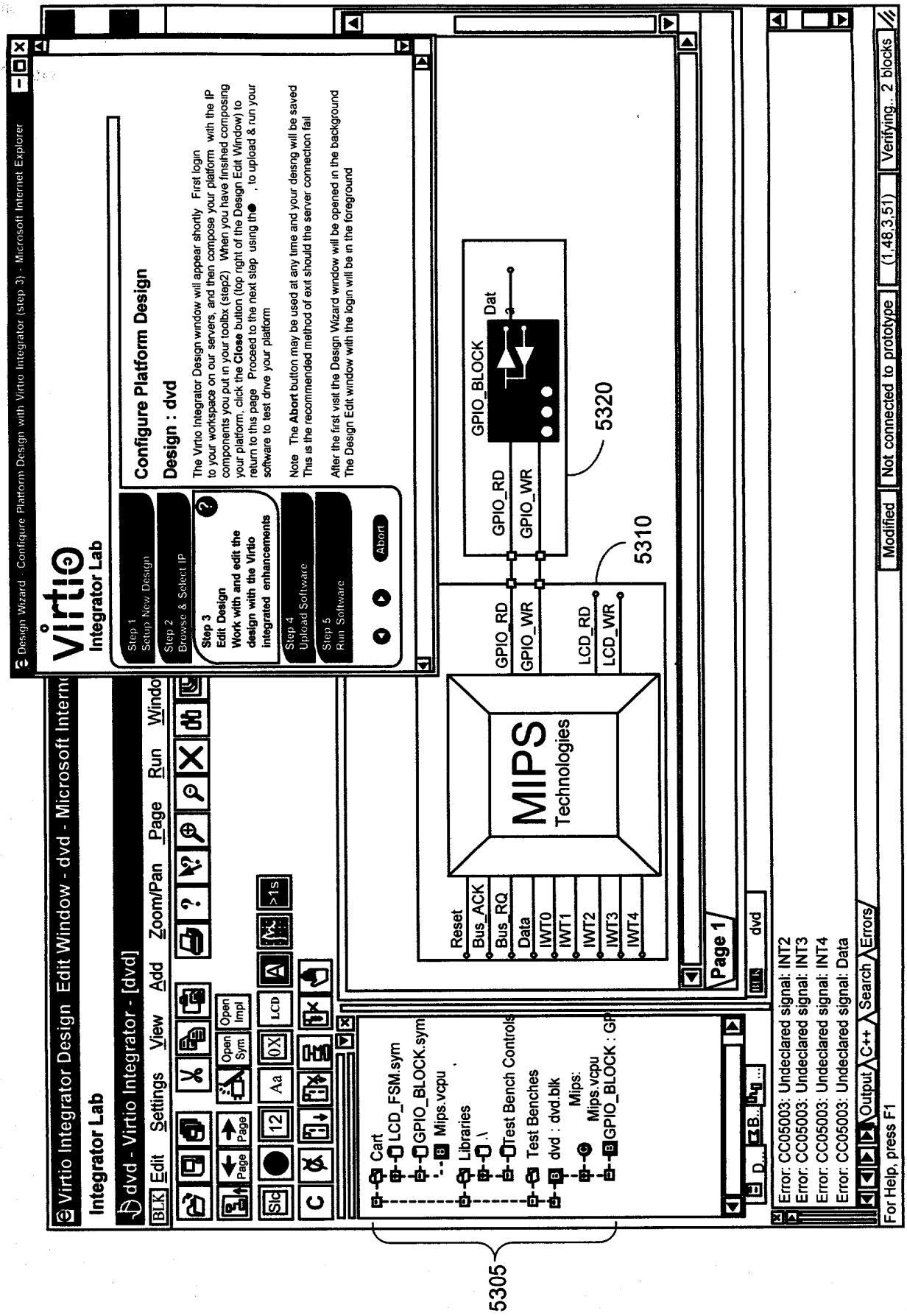
Virtio Integrator Design Edit Window - dvd - Microsoft Interne
Integrator Lab
dvd - Virtio Integrator - [dvd]
BLK Edit Settings View Add Zoom/Pan Page Run Windo
Design Wizard - Configure Platform Design with Virtio Integrator (step 3) - Microsoft Internet Explorer
Virtio
Integrator Lab
Step 1 Setup New Design
Step 2 Browse & Select IP
Step 3 Edit Design
Work with and edit the design with the Virtio integrated enhancements
Step 4 Upload Software
Step 5 Run Software
Abort
Configure Platform Design
Design : dvd
The Virtio Integrator Design window will appear shortly First login to your workspace on our servers, and then compose your platform with the IP components you put in your toolbx (step2) When you have finished composing your platform, click the Close button (top right of the Design Edit Window) to return to this page Proceed to the next step using th , to upload & run your software to test drive your platform
Note The Abort button may be used at any time and your desrng will be saved This is the recommended method of exit should the server connection fail
After the first visit the Design Wizard window will be opened in the background The Design Edit window with the login will be in the foreground
GPIO_BLOCK
Dat
GPIO_RD
GPIO_WR
5320
5310
LCD_RD
LCD_WR
MIPS
Technologies
Reset
Bus_ACK
Bus_RQ
Data
IWT0
IWT1
IWT2
IWT3
IWT4
Page 1
Cart
LCD_FSM.sym
GPIO_BLOCK.sym
Mips.vcpu
Libraries
Test Bench Controls
Test Benches
dvd : dvd.blk
Mips: Mips.vcpu
GPIO_BLOCK : GP
5305
Error: CC05003: Undeclared signal: INT2
Error: CC05003: Undeclared signal: INT3
Error: CC05003: Undeclared signal: INT4
Error: CC05003: Undeclared signal: Data
Output C++ Search Errors
For Help, press F1
Modified
Not connected to prototype
(1,48,3,51)
Verifying... 2 blocks

Fig. 53

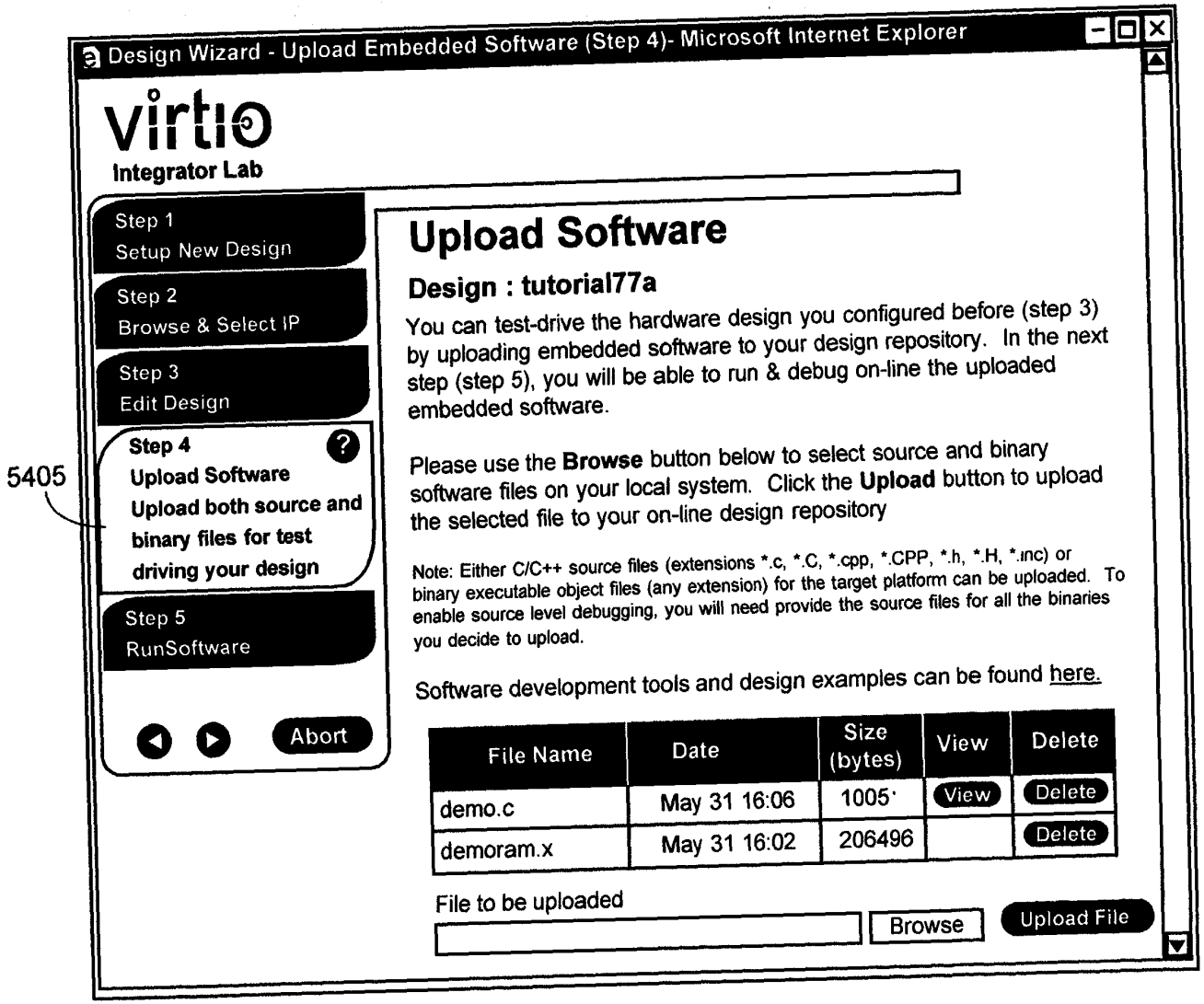

Fig. 54

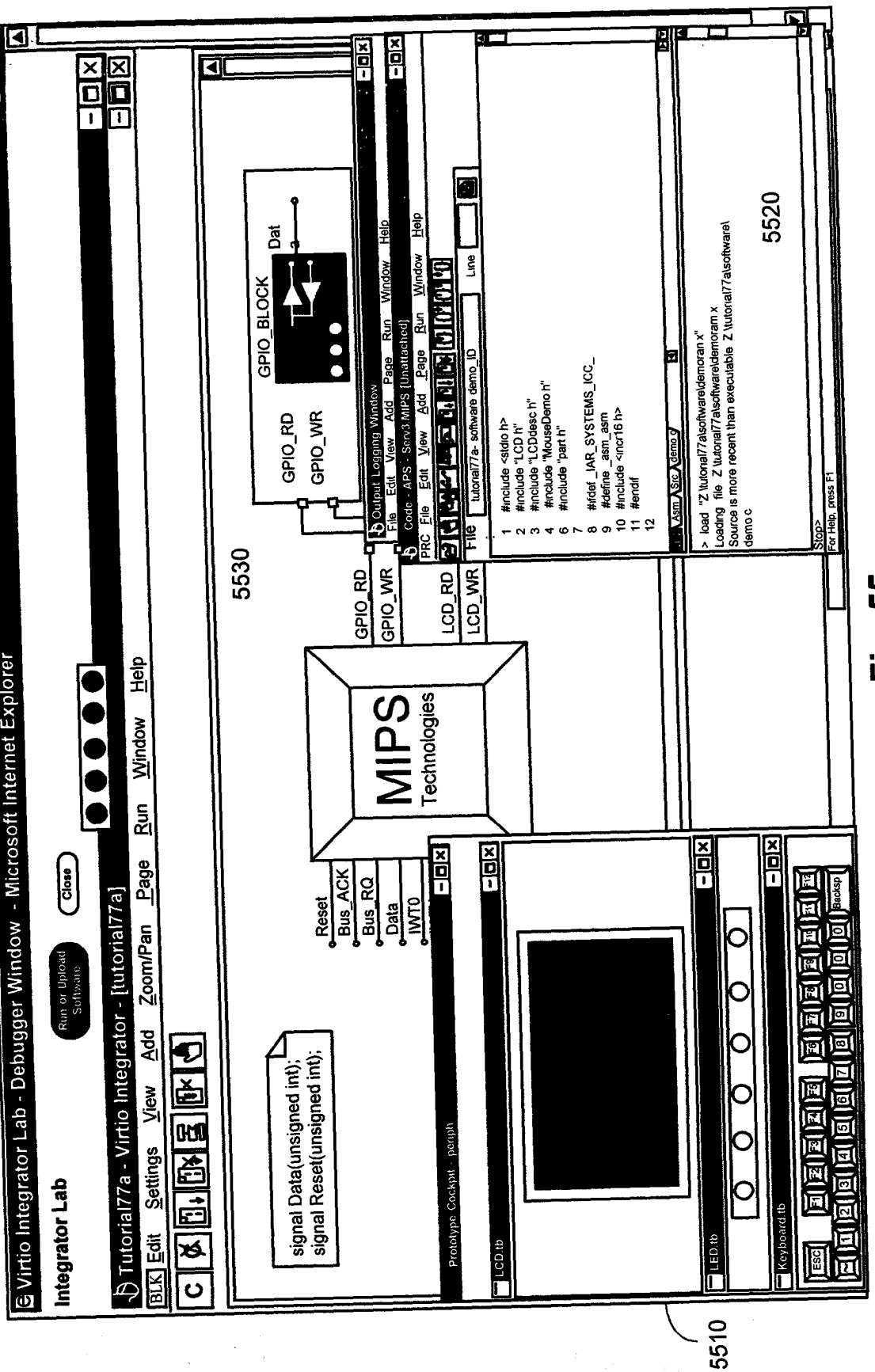
Virtio Integrator Lab - Debugger Window - Microsoft Internet Explorer
Integrator Lab
Run or Upload Software
Close
Tutorial77a - Virtio Integrator - [tutorial77a]
BLK Edit Settings View Add Zoom/Pan Page Run Window Help
signal Data(unsigned int);
signal Reset(unsigned int);
Reset
Bus_ACK
Bus_RQ
Data
IWTO
MIPS Technologies
GPIO_RD
GPIO_WR
LCD_RD
LCD_WR
GPIO_BLOCK
Dat
GPIO_RD
GPIO_WR
5530
5520
5510
Prototype Cockpit - periph
LCD.tb
LED.tb
Keyboard.tb
Output Logging Window
Code - APS - Serv3 MIPS [Unattached]
tutorial77a- software demo_ID
Line
#include <stdio.h>
#include "LCD.h"
#include "LCDdesc.h"
#include "MouseDemo.h"
#include "part.h"
#ifdef __IAR_SYSTEMS_ICC__
#define _asm_ asm
#include <ncr16.h>
#endif
Asm Src demo.g
> load \"Z:\tutorial77a\software\demoram.x"
Loading file Z:\tutorial77a\software\demoram.x
Source is more recent than executable Z:\tutorial77a\software\demo.c
Stop>
For Help, press F1

Fig. 55